SEMICONDUCTOR

PHY6202

Bluetooth Low Energy (BLE) System on Chip

Key Features

- ARM® Cortex™-M0 32-bit processor
- Memory
  - 512/256KB in-system flash memory
  - 128KB ROM
  - 138KB SRAM, all programmable retention in sleep mode
  - 8-channel DMA
- 33/19 general purpose I/O pins
  - All pins can be configured as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - 18 pins for triggering interrupt
  - 3 quadrature decoder(QDEC)
  - 6-channel PWM
  - 4-channel I2S
  - 2-channel PDM
  - 2-channel I2C
  - 2-channel SPI
  - 2-channel UART
  - JTAG
- 8-channel 12bit ADC with analog PGA
- 4-channel 32bit timer, one watchdog timer
- Real timer counter (RTC)
- Power, clock, reset controller
- Flexible power management
  - Supply voltage range 1.8V to 3.6V
  - Embedded buck DC-DC
  - Embedded LDOs
  - Battery monitor: Supports low battery detection
  - 2μA @ Sleep Mode with 32KHz RTC
  - 0.7μA @ OFF Mode(IO wake up only)
- 2.4 GHz transceiver
  - Compliant to Bluetooth 5.0, ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US) and ARIB STD-T66 (Japan)
  - Sensitivity:
    -97dBm@BLE 1Mbps data rate
    -103dBm@BLE 125Kbps data rate
  - TX Power -20 to +10dBm in 3dB steps
  - Receiver: 8mA @sensitivity level
  - Transmitter: 8mA @0dBm TX power
  - Single-pin antenna: no RF matching or RX/TX switching required
  - RSSI (1dB resolution)
- RC oscillator hardware calibrations
  - 32KHz RC oscillator automatic calibration
  - 32MHz RC oscillatorautomatic calibration
- AES-128 encryption hardware
  - AES-ECB
  - AES-CCM
- Link layer hardware
  - Automatic packet assembly
  - Automatic packet detection and validation
  - Auto Re-transmit
  - Auto ACK
  - Hardware Address Matching
  - Random number generator
- Operating temperature: -40 ℃~125℃
- RoHS Package: QFN48/ QFN32
- Applications: wearables, beacons, appliances, home and building, health and medical, sports and fitness, industrial and manufacturing, retail and payment, security, data transmission, remote control, PC/mobile/TV peripherals, internet of things (IoT)

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Table of Contents

1 Introduction

PHY6202 is a System on Chip (SoC) for Bluetooth® low energy applications. PHY6202 has 32-bit ARM® Cortex™-M0 CPU with 138KSRAM/Retention SRAM and an ultra-low power, high performance, multi-mode radio. PHY6202 can support BLE with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

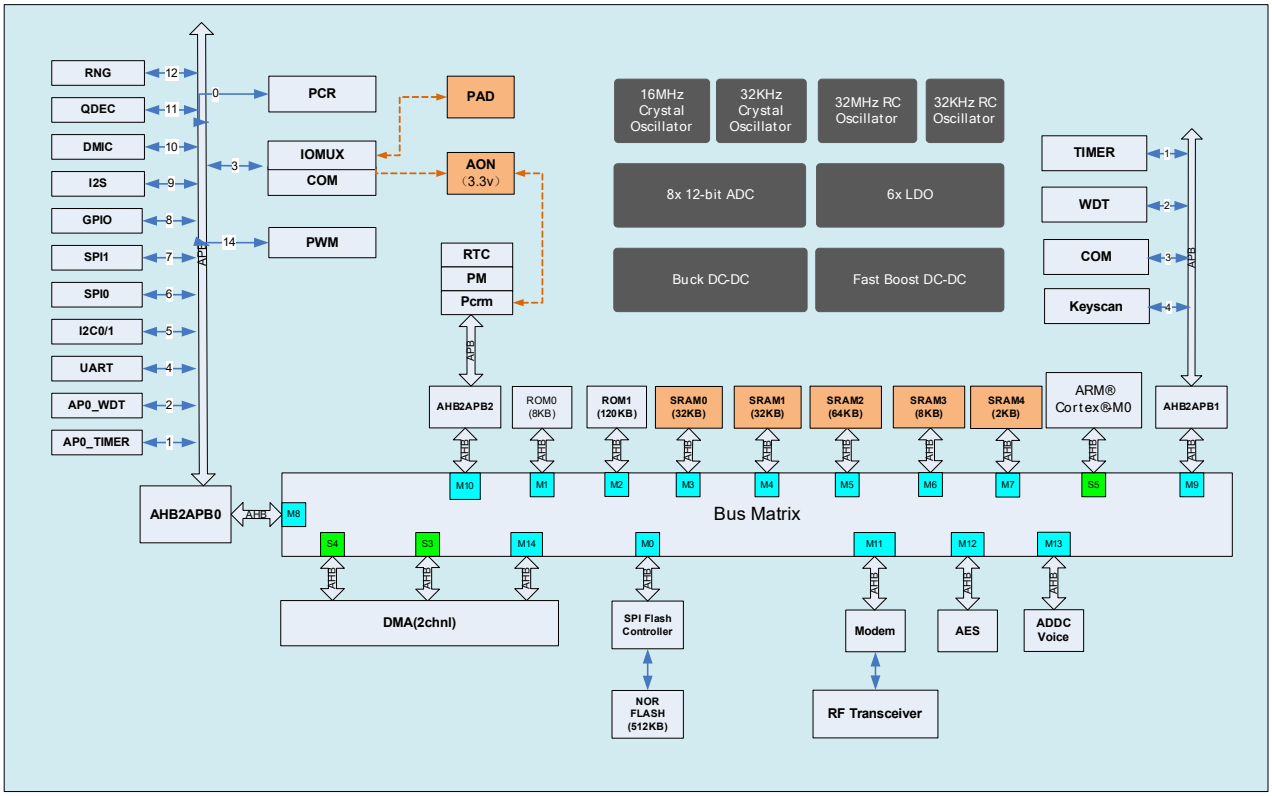

Figure 1： PHY6202 block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the different package types.

2.2.1 PHY6202 (QFN48)

2.2.1.1 Pin Assignment

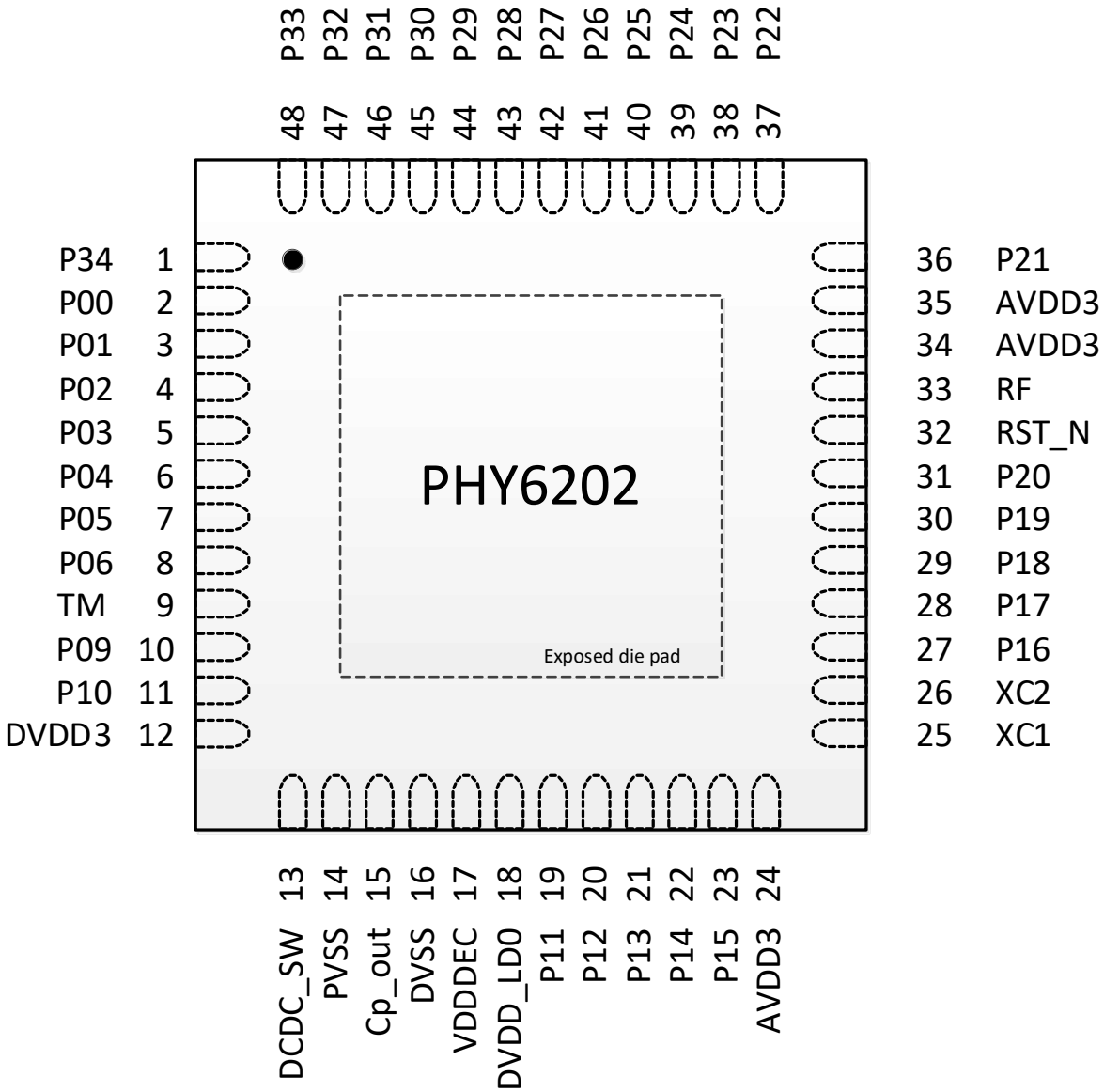

Figure 2： Pin assignment - PHY6202 QFN48 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	P34	all functions configurable
2	P00	all functions configurable/ JTAG_TDO
3	P01	all functions configurable/ JTAG_TDI
4	P02	all functions configurable/JTAG_TMS
5	P03	all functions configurable/JTAG_TCK
6	P04	all functions configurable
7	P05	all functions configurable
8	P06	all functions configurable
9	TM	Test_Mode
10	P09	all functions configurable
11	P10	all functions configurable
12	DVDD3	3V power supply for digital IO, DCDC, Charge pump
13	DCDC_SW	Buck dcdc output
14	PVSS	Buck dcdc and charge pump power vss
15	cp_out	charge pump output
16	DVSS	digital vss
17	VDDDEC	1.2V VDD_CORE, digital LDO output
18	DVDD_LDO	digital LDO input
19	P11	all functions configurable/AIO<0>
20	P12	all functions configurable/AIO<1>
21	P13	all functions configurable/AIO<2>
22	P14	all functions configurable/AIO<3>
23	P15	all functions configurable/AIO<4>
24	AVDD3	3V power supply for analog IO, bg, rcosc, etc
25	XC1	16M crystal input
26	XC2	16M crystal output
27	P16	all functions configurable/AIO<5>/32K crystal input
28	P17	all functions configurable/AIO<6>/32k crystal output
29	P18	all functions configurable/AIO<7>/PGA differential positive input
30	P19	all functions configurable/AIO<8>/PGA differential negative input
31	P20	all functions configurable/AIO<9>/Micphone bias output
32	RST_N	reset pin

33	RF	RF antenna
34	AVDD3	LNA_VDD
35	AVDD3	TRX_VDD
36	P21	all functions configurable
37	P22	all functions configurable
38	P23	all functions configurable
39	P24	all functions configurable/test_mode_select[0]
40	P25	all functions configurable/test_mode_select[1]
41	P26	all functions configurable
42	P27	all functions configurable
43	P28	all functions configurable
44	P29	all functions configurable
45	P30	all functions configurable
46	P31	all functions configurable
47	P32	all functions configurable
48	P33	all functions configurable

Table 1： Pin functions PHY6202 QFN48 package

2.2.2 PHY6202 (QFN32)

2.2.2.1 Pin Assignment

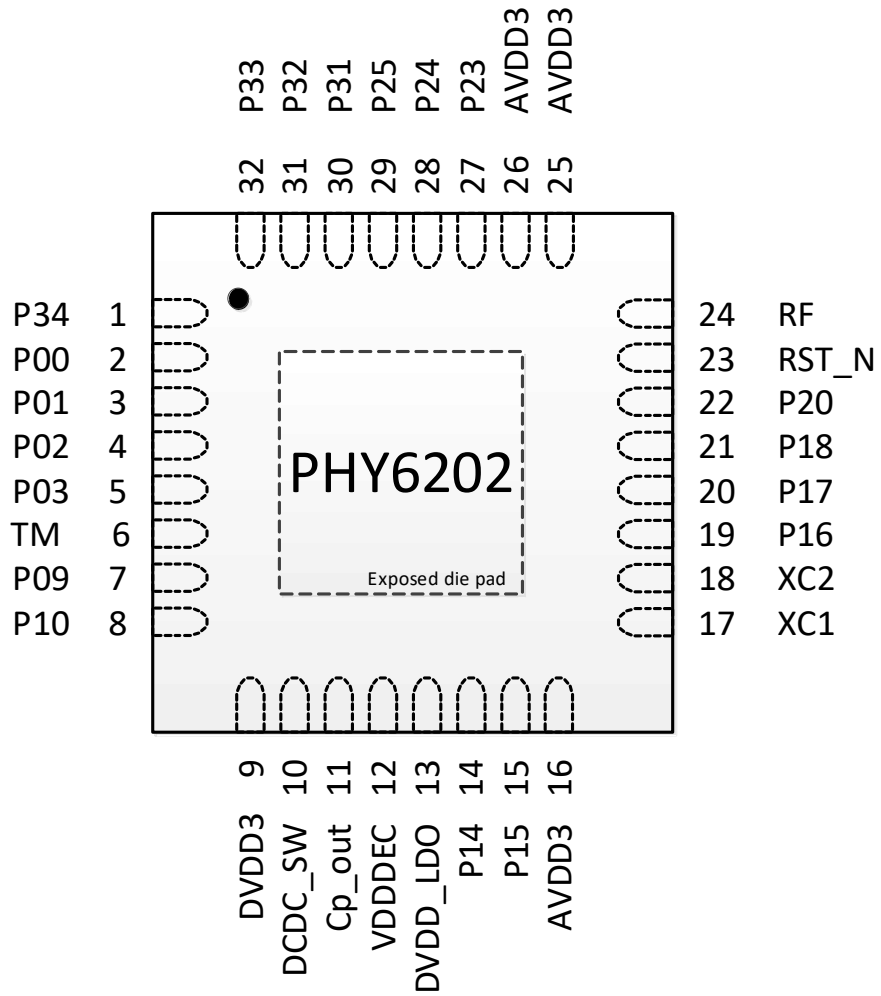

Figure 3： Pin assignment - PHY6202 QFN32 package

2.2.2.2 Pin Functions

Pin	Pin name	Description
1	P34	all functions configurable
2	P00	all functions configurable/ JTAG_TDO
3	P01	all functions configurable/ JTAG_TDI
4	P02	all functions configurable/JTAG_TMS
5	P03	all functions configurable/JTAG_TCK
6	TM	Test_Mode
7	P09	all functions configurable
8	P10	all functions configurable
9	DVDD3	3V power supply for digital IO, DCDC, Charge pump
10	DCDC_SW	Buck dcdc output
11	cp_out	charge pump output
12	VDDDEC	1.2V VDD_CORE, digital LDO output

13	DVDD_LDO	digital LDO input
14	P14	all functions configurable/AIO<3>
15	P15	all functions configurable/AIO<4>
16	AVDD3	3V power supply for analog IO, bg, rcosc, etc
17	XC1	16M crystal input
18	XC2	16M crystal output
19	P16	all functions configurable/AIO<5>/32K crystal input
20	P17	all functions configurable/AIO<6>/32k crystal output
21	P18	all functions configurable/AIO<7>/PGA differential positive input
22	P20	all functions configurable/AIO<9>/Micphone bias output
23	RST_N	reset pin
24	RF	RF antenna
25	AVDD3	LNA_VDD
26	AVDD3	TRX_VDD
27	P23	all functions configurable
28	P24	all functions configurable/test_mode_select[0]
29	P25	all functions configurable/test_mode_select[1]
30	P31	all functions configurable
31	P32	all functions configurable
32	P33	all functions configurable

Table 2： Pin functions PHY6202 QFN32 package

3 System Blocks

The system block diagram of PHY6202 is shown in **Figure 1**.

3.1 CPU

The PHY6202 has an ARM Cortex-M0 CPU. The CPU, memories, and all peripherals are connected by AMBA bus fabrics.

The ARM® Cortex™-M0 CPU has a 16-bit instruction set with 32-bit extensions (Thumb-2® technology) that delivers high-density code with a small-memory-footprint. By using a single-cycle 32-bit multiplier, a 3-stage pipeline and a Nested Vector Interrupt Controller (NVIC), the ARM Cortex™-M0 CPU makes program execution simple and highly efficient.

The CPU will play controller role in BLE modem and run all user applications. The following main features are listed below.

- Up to 48Mhz ARM Cortex™-M0 processor core.
    - Low gate count and high energy efficient.
    - ARMv6M architecture, Thumb ISA but no ARM ISA.
    - No cache and no TCM.
    - Up to 32 interrupts embedded NVIC.
    - SysTick timer.
    - Sleep/deep sleep mode.
    - Support low power WFI and WFE
- 4 32-bit general purpose timers and 1 watchdog timer (WDT).
- 120KB ROM for boot and protocol stack.
- 138KB retention SRAM for program and data.
- AHB to APB Bridge for peripherals and registers.
- Clock and reset controller.
- AHB debug access port interface and DAP ROM.
- APB interface to/from BLE modem.
- Dynamic and static clock gating to save power.
- No TRACE.

Some of these features are shared with the AP subsystem.

3.2 Memory

PHY6202 has total 128KB ROM, 138KB SRAM and up to 512KB FLASH. The physical address space of these memories is shown in **Figure 4**.

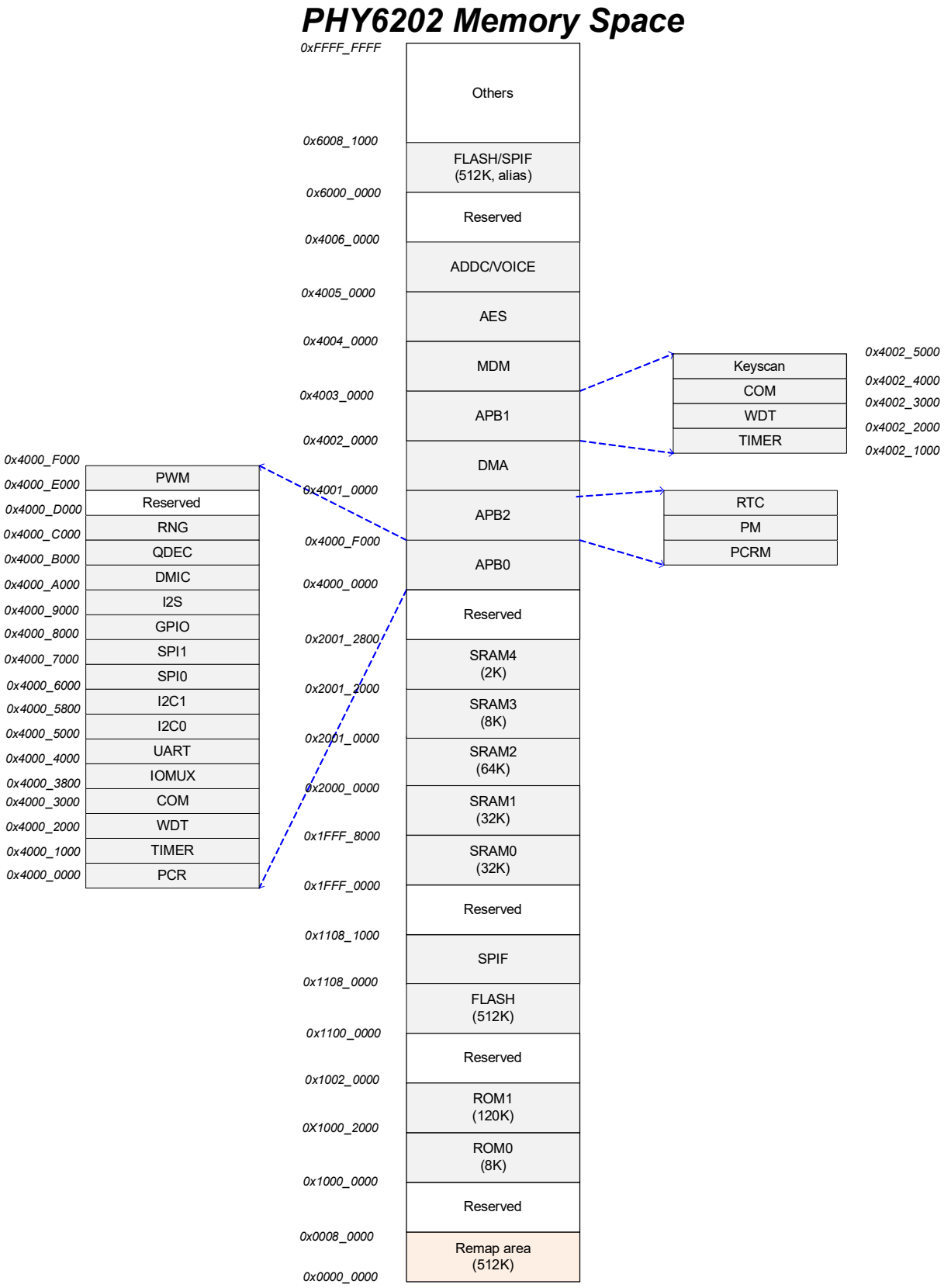

Figure 4: PHY6202 memory space

3.2.1 ROM

PHY6202 has 2 ROMs.

	SIZE	CONTENT
ROM0	8KB	Reserved
ROM1	120KB	Boot ROM for M0. Protocol stack. Common peripheral drivers.

Table 3： List of ROMs

3.2.2 SRAM

PHY6202 has 5 SRAM blocks. All 5 SRAM blocks have retention capability. which can be configured individually. All SRAM blocks can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	
SRAM1	32KB	
SRAM2	64KB	
SRAM3	8KB	
SRAM4	2KB	

Table 4： List of SRAMs

3.2.3 FLASH

PHY6202 has FLASH to provide non-volatile program and data storage. The size of the FLASH can be 256KB or 512KB. PHY6202 supports 2-wire reading.

3.2.4 Memory Address Mapping

Name	Size（KB）	Master	Physical Address	CM4 Alias	M0 Remap		
					0	1	2
ROM0	8	M0	1000_0000~1000_1FFF	0x0			
ROM1	120	M0	1000_2000~1001_FFFF		0x0		
RAM0	32	M0	1FFF_0000~1FFF_7FFF				
RAM1	32	M0	1FFF_8000~1FFF_FFFF				
RAM2	64	M0	2000_0000~2000_FFFF			0x0	
RAM3	8	M0	2001_0000~2001_1FFF				
RAM4	2	M0	2001_2000~2001_27FF				
FLASH	512	M0	1100_0000~1107_FFFF				0x0
			6000_0000~6007_FFFF				

Table 5： Memory address mapping

3.3 Boot and Execution Modes

During the boot, the ROM1 is aliased to 0x0 address. The M0 starts to execute the program from the ROM1.

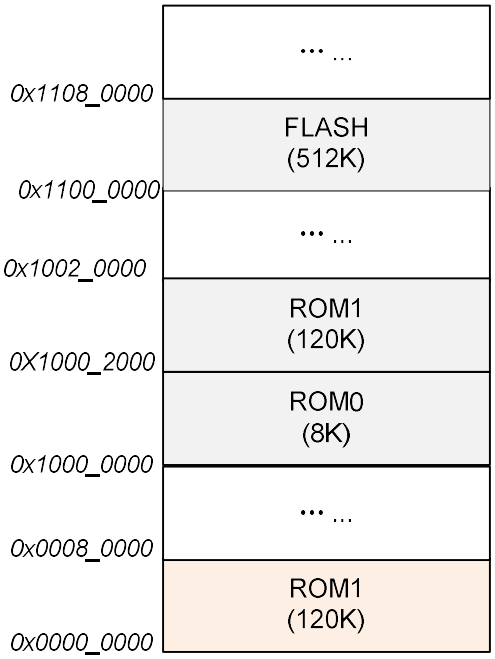

Figure 5： PHY6202 boot mode

3.3.1 Mirror Mode

The mirror mode is not tied to the chip variations. Any chip variation can use mirror mode to execute program. In the mirror mode, the program is copied from the FLASH to the SRAM, then is executed in the SRAM. For the M0 processor, one of the SRAM blocks must be aliased to 0x0 address.

3.3.2 FLASH Mode

The FLASH mode is not tied to the chip variations. Any chip variation can use FLASH mode to execute program. In the FLASH mode, the program is executed in the FLASH. For the M0 processor, the FLASH must be aliased to 0x0 address.

3.3.3 Bootloader

The bootloader in the ROM has the basic structure as shown below. The content in the FLASH should be specifically defined to allow bootloader to identify whether the FLASH content is valid, as shown in the example below. If the FLASH is valid, the ROM bootloader will put the chip in the normal mode and start normal program execution. If the FLASH is not valid, the bootloader will enter FLASH programming mode.

Address	Variable	Content
0	PRODUCT_MODE	Identify the chip mode
4	CODE_BASE	The base address of the code
8	CODE_LEN	The length of the code
C	BOOT_MODE	Identify mirror or FLASH mode

Table 6： Flash content example

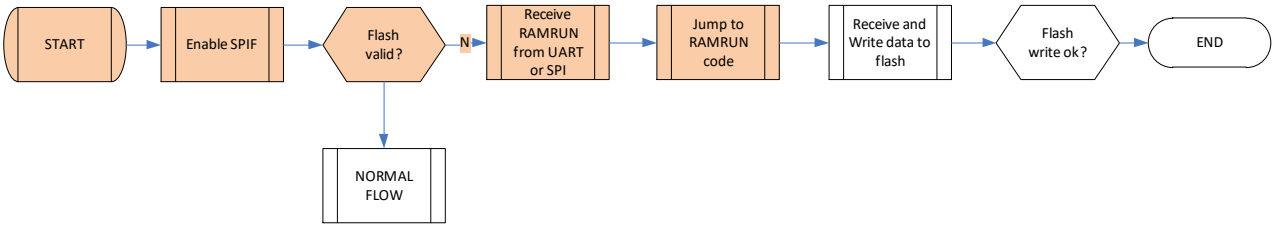

Figure6： Bootloader flow

3.4 Power, Clock and Reset (PCR)

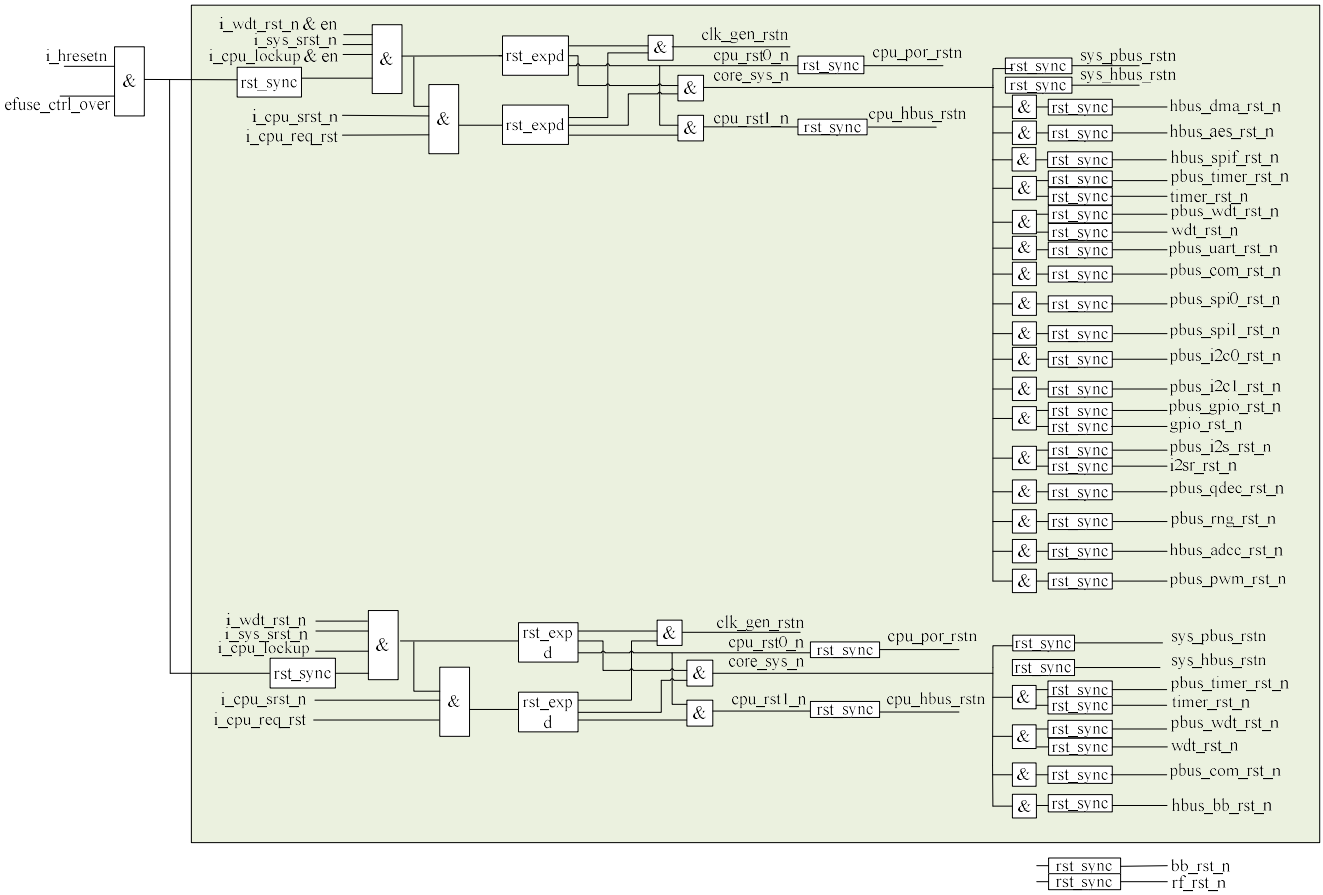

Figure 7： PHY6202 power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

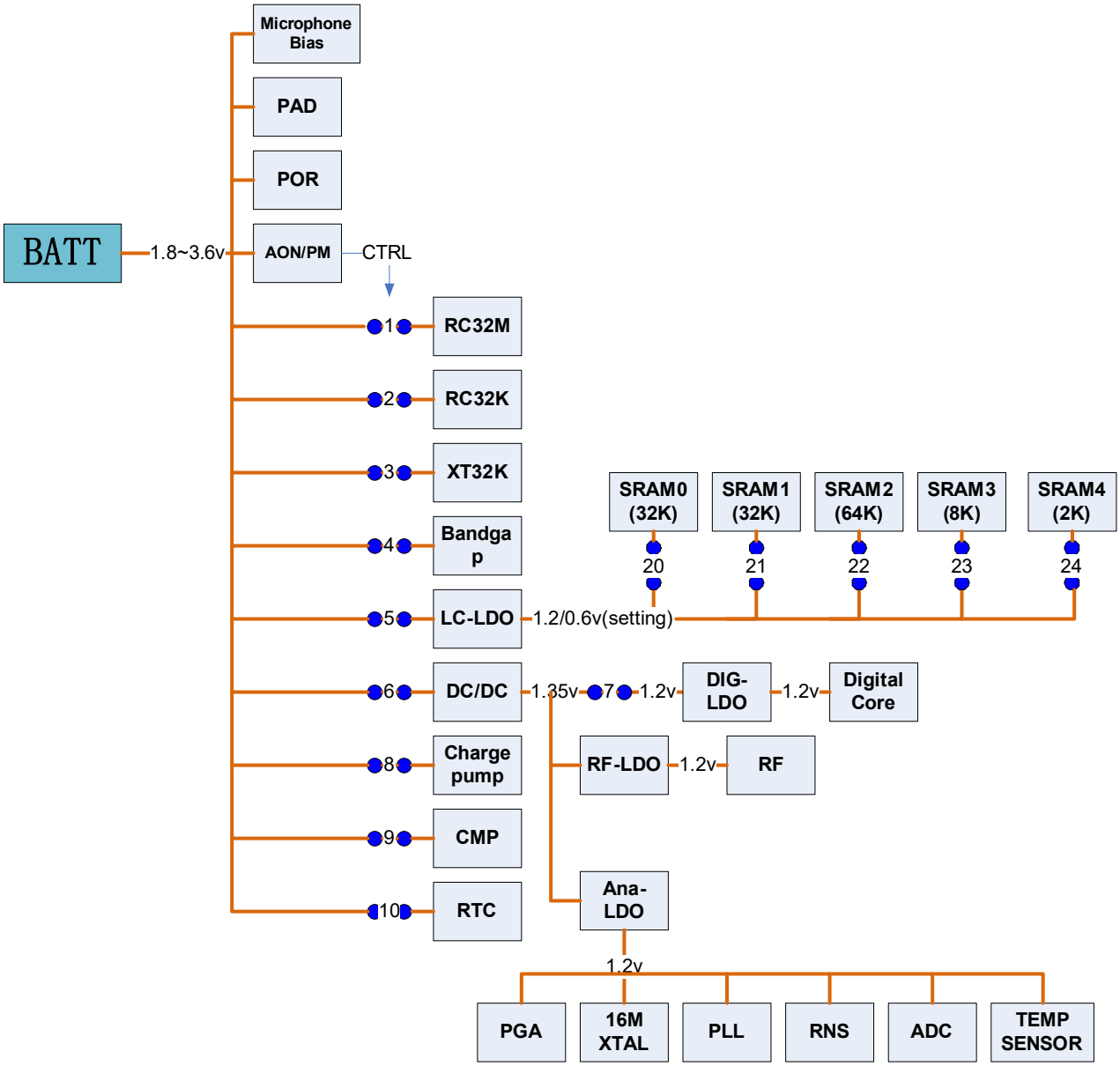

Figure 8: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

Switch	Normal	Sleep	Off
1RC32M	On	Off	Off
2RC32K	On	Optional	Off
3XT32K	On	Optional	Off
4bandgap	On	Off	Off
5LC-LDO	On	on	Off
6DC/DC	On	Off	Off
7DIG-LDO	On	Off	Off
8charge pump	On	Off	Off
9CMP	On	Optional	Off

10RTC	On	Optional	Off
20SRAM-32K	1.2v	0.6v	0
21SRAM-32K	1.2v	0.6v	0
22SRAM-64K	1.2v	0.6v	0
23SRAM-8K	1.2v	0.6v	0
24SRAM-2K	1.2v	0.6v	0

Table 7： Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include：

- IOs
- RESET
- UVLO reset

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode or FLASH mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep or off mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	M0 Interrupt Number
Reserved	0
Reserved	1
cp_timer_irq	2
cp_wdt_irq	3

bb_irq	4
kscan_irq	5
rtc_irq	6
Reserved	7
Reserved	8
timer_irq	9
wdt_irq	10
uart_irq	11
i2c0_irq	12
i2c1_irq	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
i2s_irq	17
spif_irq	18
dmac_intr	19
dmac_inttc	20
dmac_interr	21
fpidc	22
fpdzc	23
fpioc	24
fpufc	25
fpofc	26
fpixc	27
aes_irq	28
adcc_irq	29
qdec_irq	30
rng_irq	31

Table 8： Interrupts

3.8 Clock Management (CLOCK)

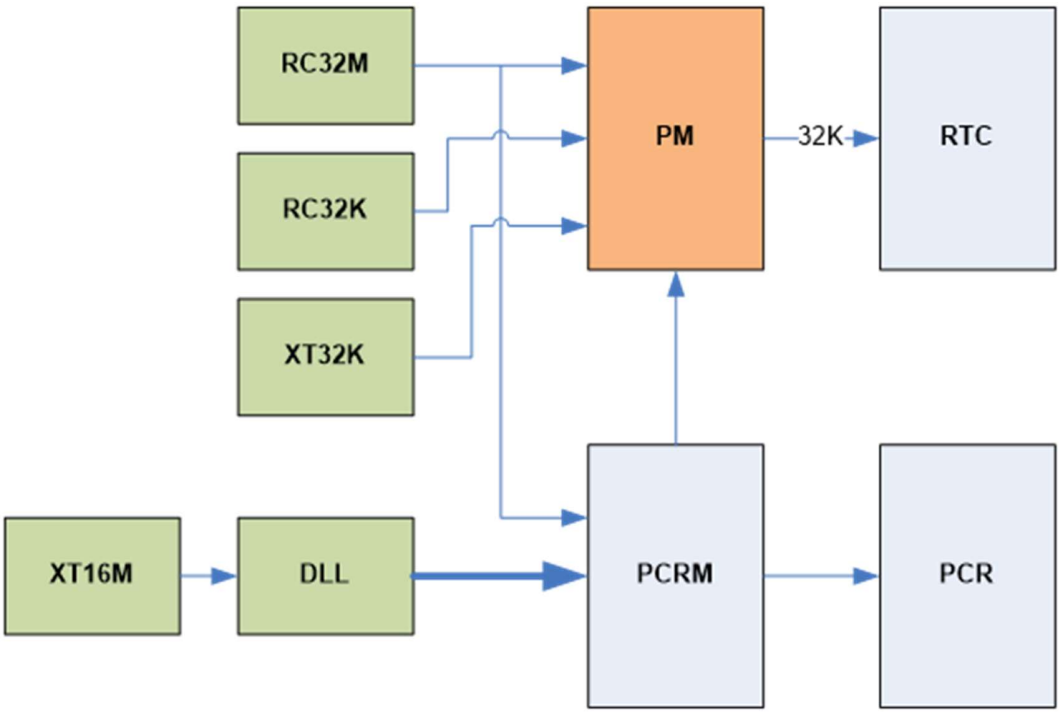

Figure 10： Clock management

There are two crystal clock sources: 16MHz crystal oscillator (XT16M) and 32.768kHz crystal oscillator (XT32k), of which the 32.768k crystal oscillator is optional. There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. If 32.768kHz crystal is not installed, RC32k oscillator would be periodically calibrated and used for RTC. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz from the XT16M clock source.

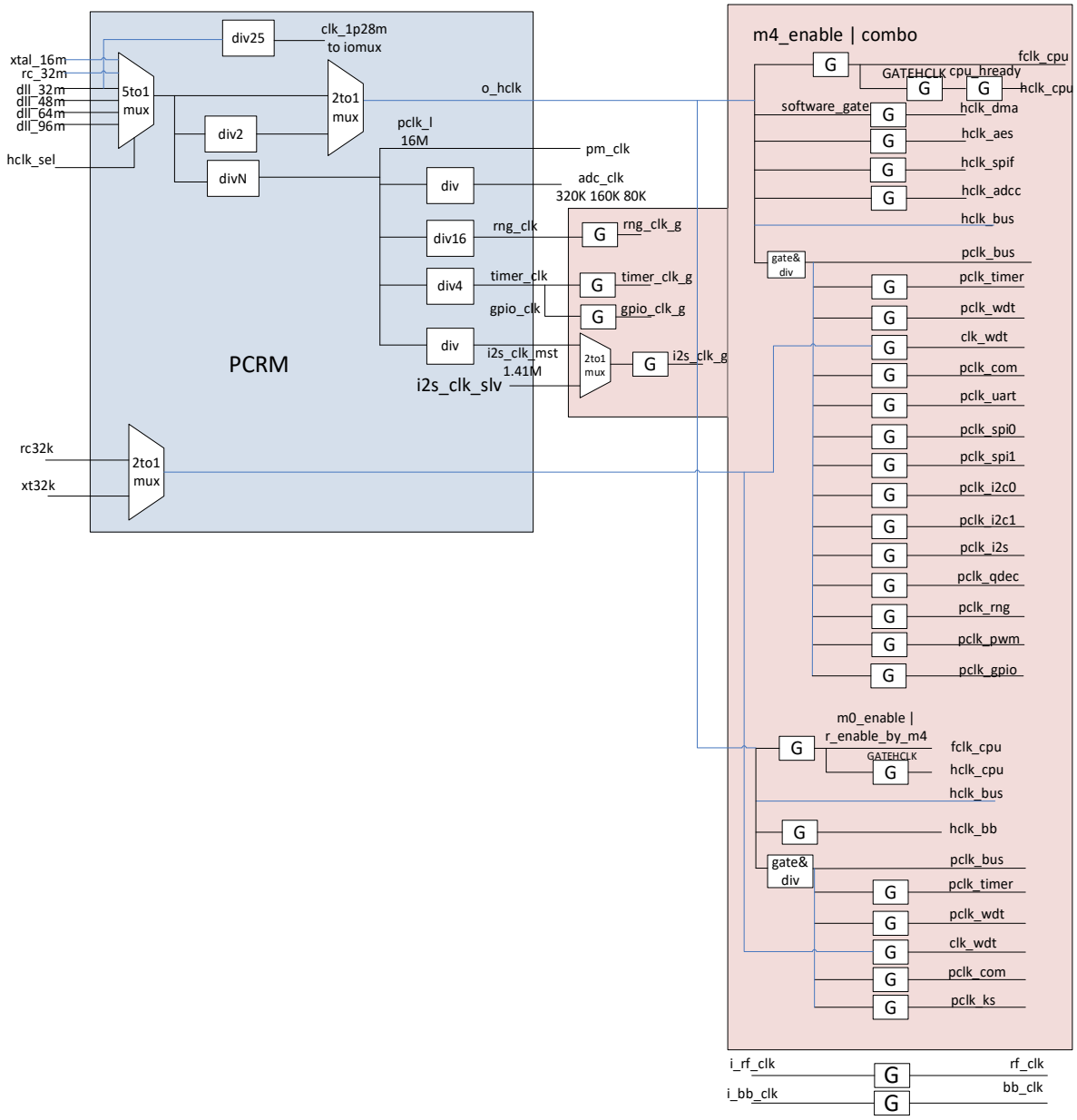

Figure11： Clock structure diagram

3.9 GPIO

The Flexible general purpose I/O is organized as two PORTs. Each port has bi-direction 18 bit line, e.g., GPIO_PORTA[17:0] and GPIO_PORTB[17:0]. Only PORTA has debounce logic.

- All pins can be configured as serial interface and programmable IO MUX function mapping
- All pins can be configured for wake-up
- 18 pins with trigger interrupt
- Three Quadrature Decoder(QDEC)
- 6 channel PWM

- 4 channel I2S, 2 channel PDM, 2 channel I2C, 2 channel UART, 2 channel SPI, JTAG

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE) protocol implementations.

- General modulation format
  - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
  - OQPSK with half-sine shaping
  - On-air data rates
    - 125kbps/250kbps/500kbps/1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +10dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
  - -103dBm@125Kbps GFSK
  - -98dBm@500Kbps GFSK
  - -97dBm@1Mbps BLE
  - -94dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 24-bit SysTick system timer, that extends the functionality of both the processor and the NVIC.When present, the NVIC part of the extension provides:

- A 24-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.
- See the ARMv7-M ARM for more information.

General purpose timers are included in the design. This timer is Synopsys DW_apb_timer. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24 bit COUNTER, 12 bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128 bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Random Number Generator (RNG)

The Random Number Generator (RNG) generates true non-deterministic random numbers based on internal thermal noise. These random numbers are suitable for cryptographic purposes. The RNG does not require a seed value.

4.6 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.7 SPI (SPI)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI wrapper contains one SPI master and one SPI slave. There are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
1	0	SPI1 is master mode when set
0	0	SPI0 is master mode when set

Table 10： PERI_MASTER_SELECT Register bit definition (base address = 0x4002_302C)

4.8 I2C (I2c0, I2c1 Two Independent Instances)

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.9 I2S

I2S wrapper contains one I2S master and one I2S slave. There are logically exclusive. Only one block is alive at a time. The operation mode for master mode and slave mode is controlled by PERI_MASTER_SELECT Register in COM block.

bit	Reset value	Definition
3	0	I2S1 is master mode when set
2	0	I2S0 is master mode when set

Table 11： PERI_MASTER_SELECT Register bit definition (base address = 0x4002_302C)

4.10 UART (UART)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking

and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of board space and signal routing.

4.11 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.12 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is upo the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automode keyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.13 Analog to Digital Converter (ADC) & PGA

The 12bit ADC has total 10 inputs. Among them, two PGA inputs are differential path. The other eight inputs can be programmed to four pair differential inputs or eight single-ended inputs.Sampling time of each ADC channel can be independently programmed from 1.56uS to up to 25uS. There is an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

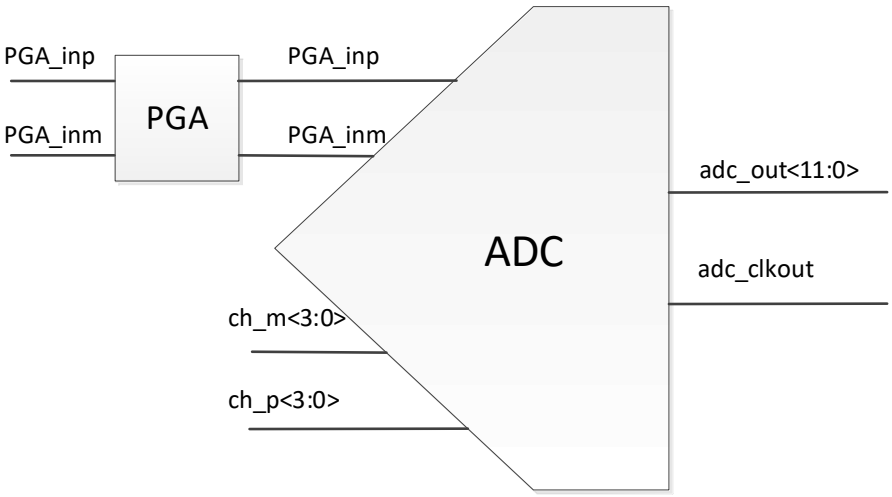

Figure 12： ADC

4.13.1 PGA Path

The PGA provides 42dB gain range from 0dB to 42dB in 3dB steps.

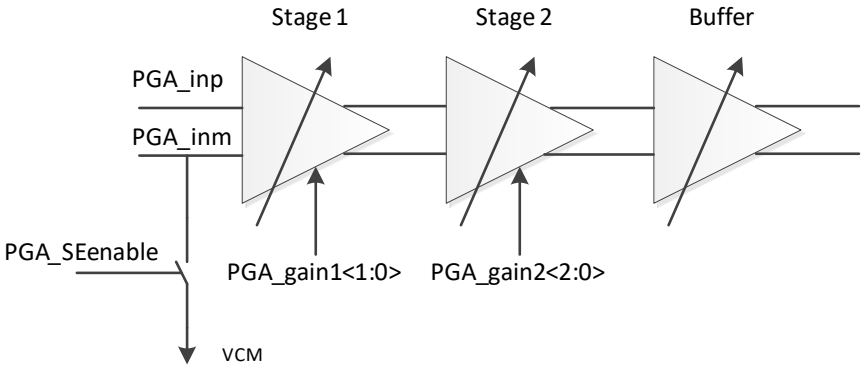

Figure 13： PGA path

pga_gain1<1>	pga_gain1<0>	Stage1 gain (dB)	pga_gain2<2>	pga_gain2<1>	pga_gain2<0>	Stage2 gain (dB)
0	0	0	0	0	0	0
0	1	12	0	0	1	3
1	0	24	0	1	0	6
			0	1	1	9
			1	0	0	12
			1	0	1	15
			1	1	0	18

Table 12： PGA gain

Set PGA_SEenable to “1”, PGA will be set to Single-ended mode by pulling the PGA into its Common-mode voltage.

4.13.2 ADC Path

The ten ADC input channels can be configured by programming their corresponding registers. Their configurations including sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, can be programmed based on following register table.

ADC_CTL0		Register Description
[31:16]	ch_tempsense_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.
[15:0]	ch_pga_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.

ADC_CTL1		Register Description
[31:16]	ch0_n_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.
[15:0]	ch0_p_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.

ADC_CTL2		Register Description
[31:16]	ch1_n_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.
[15:0]	ch1_p_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.

	ADC_CTL3	Register Description
[31:16]	ch2_n_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.
[15:0]	ch2_p_config	channel config: [3:0] sample time, for max rate 320k: 2T to 32T, step 4T; for max rate 256k, 3T to 33T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1.

Table 13： ADCchannel configurations

There is also a register to configure the overall ADC controller state, including sampling clock frequency, ADC conversion time, sampling rate base and manual (override) or auto mode. As described by the following register table.

0x7C	ADC_CTL4	Register Description
[31:16]	reserved	
[15:5]	reserved	
[4]	adc_ctrl_override	override adc_ctrl back to static: 1, override
[3]	adc_tconv_sel	adc conversion time sel: 0: 1.56us, 1: 2.34us
[2:1]	adc_clk_sel	Override mode clksel: 00: 80k, 01: 160k, 10: 320k
[0]	max_rate_256k_320k	max rate base: 0, 256k, 1, 320k

Table 14： ADCoverall configurations

4.13.3 ADC Channel <3:0> Connectivity

temp sensor outm	ch_m<0>
temp sensor outp	ch_p<0>
aio<0>	ch_m<1>
aio<1>	ch_p<1>
aio<2>	ch_m<2>
aio<3>	ch_p<2>
aio<4>	ch_m<3>
aio<5>	ch_p<3>

Table 15： ADC channel connectivity

Aio<5:0> and PGA inputs(pga_inp&pga_inm) can be selected through an analog Mux by programming aio_pass<7:0> or aio_attn<7:0>.

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which PHY6202 can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the PHY6202.**Table16**specifies the absolute maximum ratings for PHY6202.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
DEC			1.32	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		2	
ESD HBM	Human Body Model Class 2		4	kV
ESD CDMQF	Charged Device Model (QFN48, 7x7 mm package)		750	V
Flash memory				
Endurance			20 000	write/erase cycles
Retention			10 years at 40 °C	
Number of times an address can be written between erase cycles			2	times

Table 16: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that PHY6202 can operate within as defined in **Table 17**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	125	°C

Table 17： Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	with internal DC-DC @3V		8		mA
Rx Only	with internal DC-DC @3V		8		mA

Table 18： Radio current consumption

7.2 Transmitter Specification

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			10		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
OBW for GFSK 500Kbps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
OBW for GFSK 125bps	20dB occupy-bandwidth for GFSK modulation 2Mbps		1100		KHz
Error Vector Measure	Offset EVM for OQPSK modulation		0.02		
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 19： Transmitter specification

7.3 Receiver Specification

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-97		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 20： RX BLE 1Mbps GFSK

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-94		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB

Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 21： RX BLE 2Mbps GFSK

7.3.3 RX 500Kbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-98		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-4		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/-1MHz, 37 Byte BER=1E-3		10		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/-2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/-3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/-4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		24		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte Ber=1E-3		-19		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 22： RX 500Kbps GFSK

7.3.4 RX 125Kbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-103		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-1		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/-1MHz, 37 Byte BER=1E-3		-11		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/-2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/-3MHz, 37 Byte BER=1E-3		50		I/C dB

Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/-4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		28		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-18		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 23： RX 125Kbps GFSK

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 24： RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus (ARM bus standard)
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus (ARM bus standard)
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port (ARM bus standard)
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SWD	Serial Wire DAP (ARM bus standard)
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 25： Glossary

9,Ordering information

Part No.	Package	Packing	MOQ(PCS)
PHY6202AAQA	QFN32	Tray	490
	QFN32	Tape&Reel	4500
PHY6202AAQB	QFN48	Tray	416 or 260
	QFN48	Tape&Reel	3000

10,Chip Marking