ATS3015P Datasheet

Actions® ATS3015P™ QFN32

Bluetooth Audio Solution

Low Power Solution for
Portable & Wireless
Audio Applications
Headphone and Earphone

RISC32 core Single-chip
Bluetooth 5.3

Version: V1.3

2021-11-12

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Revision History

Date	Revision	Description
2020-10-20	V1.0	Initial version
2020-12-17	V1.1	Add GPIO register description
2021-8-26	V1.2	1. Upgrade Bluetooth version to BT5.3 2. Upgrade HFP Profile version to V1.8
2021-11-12	V1.3	1. Add description of chip mark 2. Add reflow solder Information

1 Introduction

1.1 Overview

Actions' ATS3015P is a highly integrated single-chip Bluetooth Audio solution. Targeting at Bluetooth headsets and earphones market, ATS3015P satisfies the market requirements with high performance, low cost and low power consumptions.

ATS3015P adopts RISC32 core architecture. Large capacity RAM is embedded to meet different Bluetooth applications. ATS3015P supports decoding Bluetooth A2DP audio and loading sound effects simultaneously, supports Bluetooth handfree calls with microphone AEC and noise reduction.

ATS3015P integrates Bluetooth controller support BT5.3 and compliant with BT5.2/5.0/4.2/4.2 LE/4.0 Bluetooth specification, and supports dual mode (BR/EDR + Low Energy Controllers). The links in BR/EDR and LE can be active simultaneously.

ATS3015P take special methods at power optimization, especially for various applications scenarios, including sniff, Bluetooth idle, Bluetooth playing and call modes. Embedded PMU supports power optimization and provide long battery life. The competitive advantages of ATS3015P are high music and call qualities with low power and BOM, which lays the foundation for our goal at high-end market.

In addition, user-friendly configuration tools and the development board (DVB) kits are available to provide easy interface to configure product behavior or specification in the engineering development phase based on ATS3015P chip platform. The mass-production (MP) tool kits, comprising golden hardware and MP software, can provide a simple and flexible manufacturing procedure with ATS3015P chipsets.

Above all, ATS3015P completes total solutions provides a fast and highly reliable development path with a very competitive BOM, making it the ideal choice for highly integrated and optimized Bluetooth audio products.

1.2 Key Features

System

- High performance 32bit RISC processor Core
- Internal 216K RAM for data and program
- Built in 32KB SPI Cache that can be used for data RAM storage if it isn't used as Cache
- Internal ROM for firmware implementation
- Internal 8M bits SPI serial Flash for custom defined software
- Support 24MHz OSC with on-chip PLL
- Fully configurable PEQ, up to 14 segments
- Support for echo cancellation
- Support ACTIONS single microphone noise reduction (ENC-S3.0)
- Support for wind noise reduction
- Support for packet loss concealment
- Support for voice prompt

Bluetooth

- Fully compatible with Bluetooth core specification 5.3
- Integrated T/R switch and balun
- Bluetooth Dual Mode support: Simultaneous LE and BR/EDR
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link with CVSD/mSBC
- AFH and PTA collaborative support for WLAN/Bluetooth coexistence
- ATWS two earphones can switch between master and slave at will
- Supports multi link in ATWS mode
- Support for SBC & AAC Bluetooth audio transmission format
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.8
- LE Data Packet Length Extension
- LE 2M PHY
- Channel Selection Algorithm #2

RF Performance

- Max transmitting output power: 10dBm
- Typical receiving sensitivity (Classic mode): -95dBm@GFSK, -94dBm@π/4 DQPSK, -88dBm@8DPSK modulation
- Typical receiving sensitivity (BLE mode): -99dBm@BLE 1M, -96dBm@BLE 2M

Audio

- Build in mono 16-bits input sigma-delta ADC, SNR 85dB (typ.), THD+N -81dB (typ.)
- ADC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48kHz
- Supports mono input analog microphone
- Supports two digital microphones
- Build in stereo 20-bits input sigma-delta DAC, SNR (A-Weighting) 101dB (typ.), Noise < 6uV, DR 92dB (typ.), THD+N -85dB (typ.)
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48k/96kHz
- Build in stereo 20mW PA for headphone
- Support I2S TX with master mode, sampling rate 8~96KHz
- Support I2S RX, sampling rate 8~48KHz

Power Management

- Operating voltage: I/O 3.1V, Core 1.1V
- Supports Li-Ion battery and 5V power supply
- Supports 5V power supply plugged in reset
- Integrated linear battery charger up to 300mA charging current
- Integrated 10-bits SARADC for battery voltage monitor, temperature monitor and wire-controller
- Integrated DC-DC buck converter, which can be switch to LDO mode
- Supports DC5V insertion detection
- Supports DC5V pull out detection
- Supports communication with charger box through power line
- Low Power Consumption:
  A2DP ATWS: 5.8mA(Min.)@Vbat
  HFP ATWS: 8.5mA(Min.)@Vbat, single microphone
  Typical Sniff Current: 260μA@500ms
  Deep sleep: <1μA@Vbat

Physical Interfaces

- Support 10 GPIO
- Support 10-bits SARADC
- Support 5 PWM for lamp controller
- Serial Interface: SPI, UART*2, TWI*2

Package

- QFN-32 (4*4*0.75mm, Pitch 0.4mm)

1.3 Application Diagram

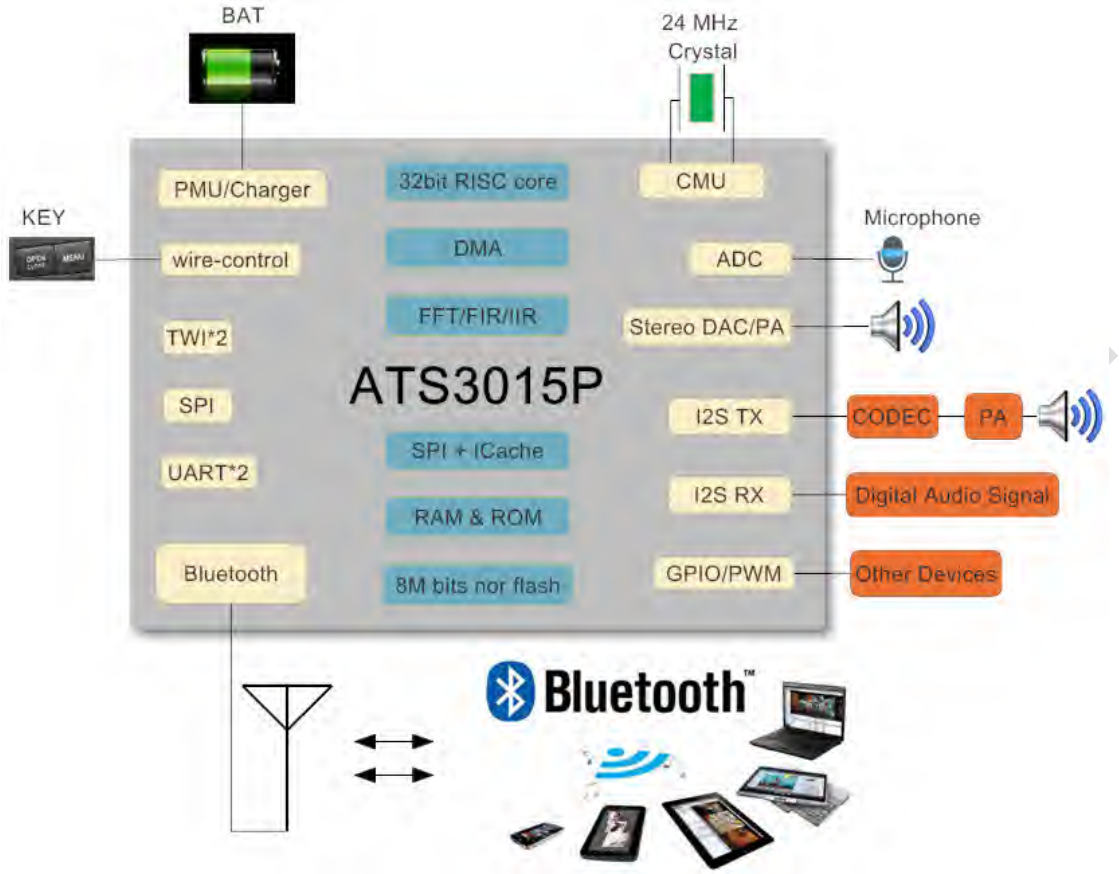
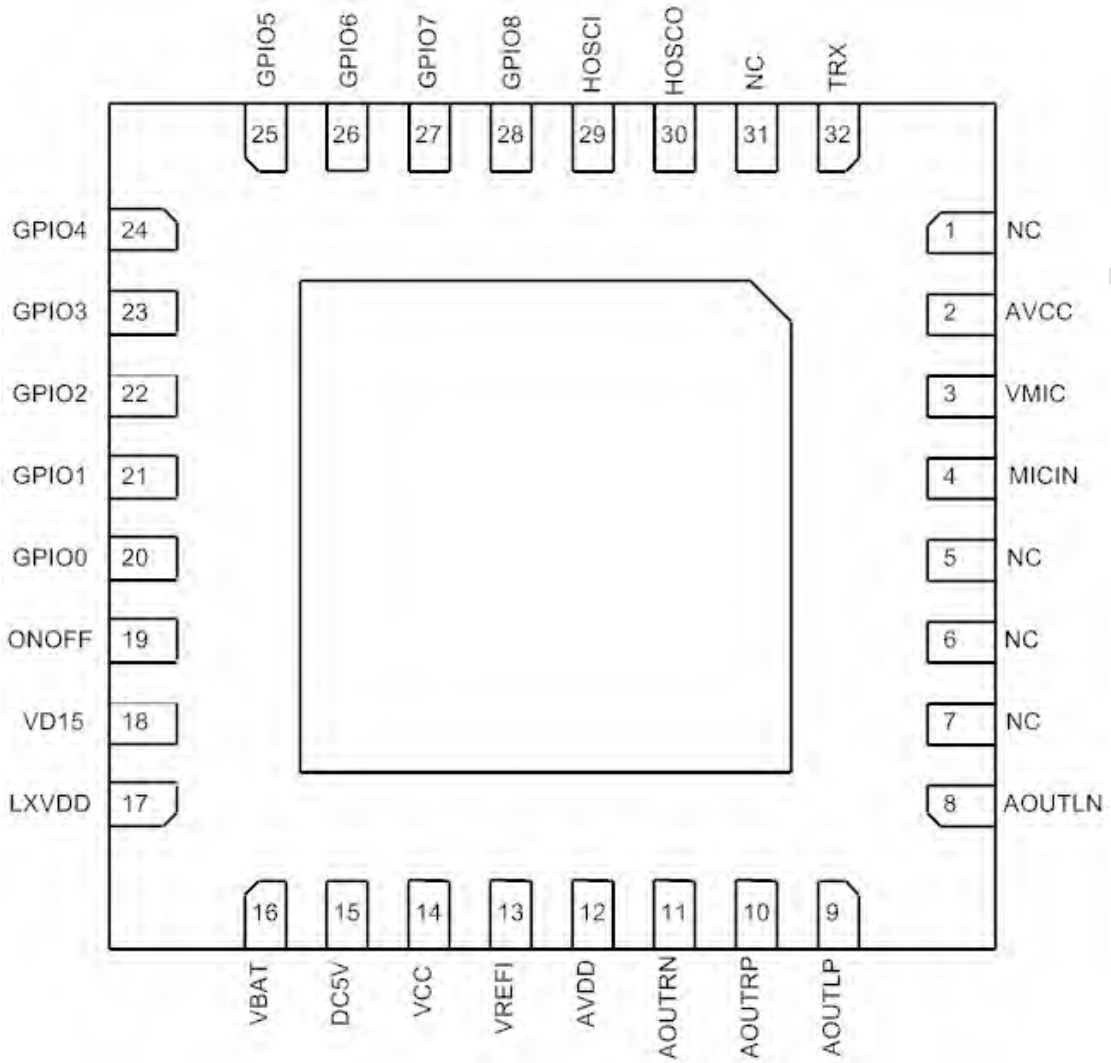


Figure 1-1 ATS3015P Application Diagram

1.4 Pin Assignment and Descriptions

1.4.1 Pin Assignment



1.4.2 Pin Description

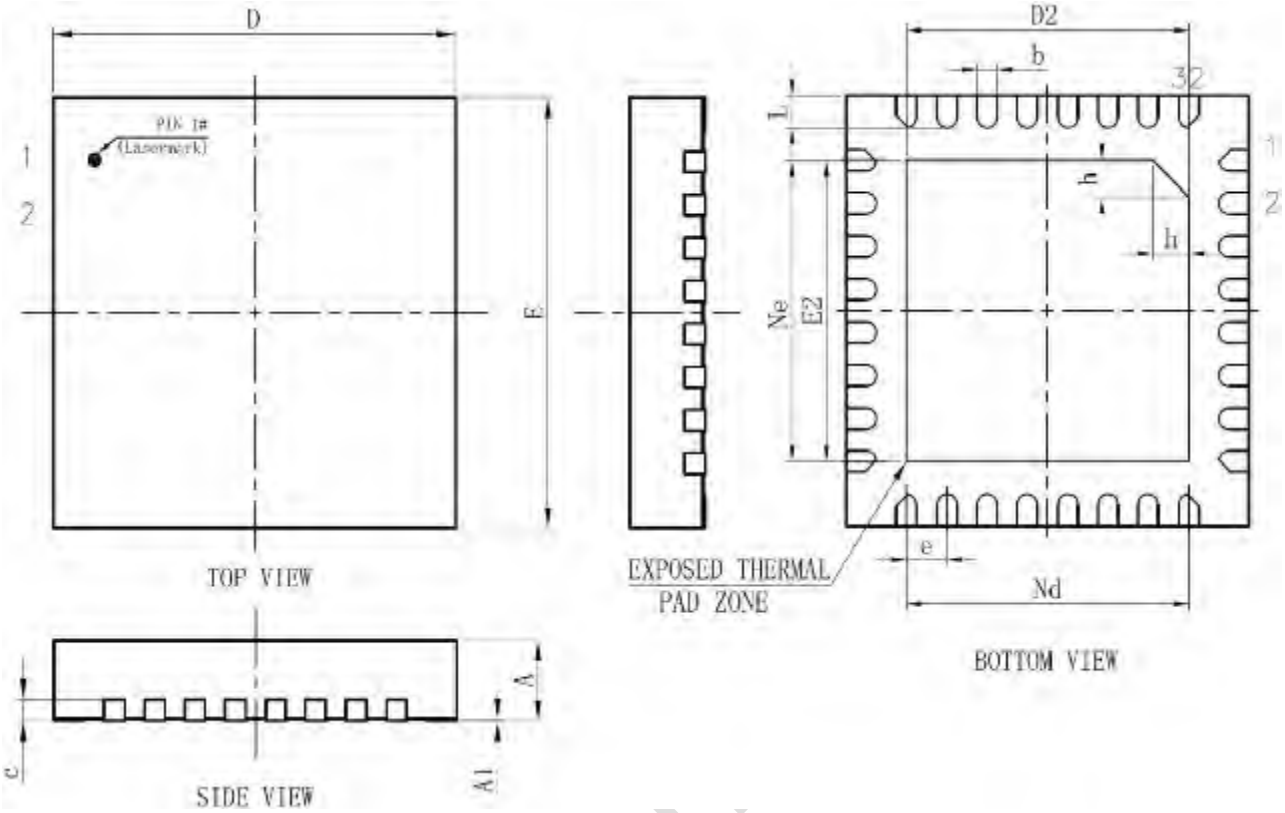
Pin No.	Pin Name	Function Multiplex	IO Type	PAD Drive Level	GPIO Initial State	Description
1	NC					
2	AVCC		PWR			2.95V voltage
3	VMIC	GPIO9 PWM3 SIRQ TWI0_SDA DMIC_CLK UART0_RX TWI1_SDA	DIO	2/4/8/10 mA	Z	VMIC(MIC power) or General purpose I/O
4	MICIN		AI			Microphone input
5	NC					
6	NC					
7	NC					
8	AOUTLN		AIO			Left channel of AUDIO Analog output
9	AOUTLP		AIO			
10	AOUTRP		AIO			Right channel of AUDIO Analog output
11	AOUTRN		AIO			
12	AVDD		PWR			1.2V voltage
13	VREFI		PWR			Reference Voltage input
14	VCC		PWR			3.1V voltage
15	DC5V		PWR			5.0V Voltage
16	VBAT		PWR			Battery Voltage input.
17	LXVDD		PWR			LXVDD
18	VD15		PWR			1.5V voltage
19	ONOFF		PWR			ON/OFF reset signal
20	GPIO0	SARADC UART0_TX UART1_TX TWI1_SDA	DIO	2/4/8/10 mA	Z	General purpose I/O
21	GPIO1	PWM0 UART0_TX TWI0_SCL	DIO	2/4/8/10 mA	Z	General purpose I/O
22	GPIO2	PWM1 UART0_RX TWI0_SDA DMIC_CLK	DIO	2/4/8/10 mA	Z	General purpose I/O
23	GPIO3	PWM2 UART0_CTS UART0_TX I2STX_MCLK I2SRX_MCLK TWI1_SCL	DIO	2/4/8/10 mA	Z	General purpose I/O
24	GPIO4	PWM3 UART0_RTS UART0_TX UART1_RX I2STX_LRCLK I2SRX_LRCLK	DIO	2/4/8/10 mA	Z	General purpose I/O
25	GPIO5	PWM4	DIO	2/4/8/10	Z	General purpose I/O

		SPI1_CLK UART1_CTS I2STX_BCLK I2SRX_BCLK		mA		
26	GPIO6	PWM0 SIRQ TEMPADC UART1_RTS SPI1_SS I2STX_DOUT I2SRX_DIN	DIO	2/4/8/10 mA	Z	General purpose I/O
27	GPIO7	PWM1 TWI0_SCL DMIC_DAT SPI1_MOSI	DIO	2/4/8/10 mA	Z	General purpose I/O
28	GPIO8	PWM2 SARADC DMIC_CLK TWI0_SDA TWI1_SCL SPI1_MISO	DIO	2/4/8/10 mA	Z	General purpose I/O
29	HOSCI		AI			24MHz clock input
30	HOSCO		AO			24MHz clock output
31	NC					
32	TRX		RF			Bluetooth antenna IO
33	EPAD		GND			Exposed pad as ground

Note:

1. *Z: high resistance.*
2. *Built-in two pull-up (100kΩ/10kΩ) and one pull-down (100kΩ) configurable resistance for the GPIO pin.*

1.4.3 Package Dimensions



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.70	2.80	2.90
e	0.40BSC		
Ne	2.80BSC		
Nd	2.80BSC		
E	3.90	4.00	4.10
E2	2.70	2.80	2.90
L	0.25	0.30	0.35
h	0.30	0.35	0.40

2 Bluetooth

2.1 Features

- Fully compatible with Bluetooth core specification 5.3
- Integrated T/R switch and balun
- Bluetooth Dual Mode support: Simultaneous LE and BR/EDR
- Supports AFH to dynamically detect channel quality to improve transmission quality
- Supports all packet types in basic rate and enhanced data rate
- Supports SCO/eSCO link with CVSD/mSBC coding
- AFH and PTA collaborative support for WLAN/Bluetooth coexistence
- ATWS two earphones can switch between master and slave at will
- Supports multi link in ATWS mode
- Support for SBC & AAC Bluetooth audio transmission format
- Compatible with AVRCP Profile V1.6
- Compatible with A2DP Profile V1.3
- Compatible with HFP Profile V1.8
- LE Data Packet Length Extension
- LE 2M PHY
- Channel Selection Algorithm #2

2.2 Bluetooth RF Performance

- Max transmitting output power: 10dBm (typical value)
- Bluetooth receiving sensitivity up to (Classic mode): -95dBm@GFSK, -94dBm@π/4 DQPSK, -88dBm@8DPSK modulation
- Bluetooth receiving sensitivity up to (BLE mode): -99dBm@1Mbps, -96dBm@2Mbps

3 Processor Core

- 160MHz RISC32 processor Core
- 32-bit Address and Data Paths
- RISC32-Compatible Instruction Set
- RISC32 Enhanced Architecture (Release 2) Features
- RISC16e™ Code Compression

4 Memory Controller

The memory controller provides dynamically allocated ring buffers that hold the data that is in transit between the host and the air. The dynamic allocation of memory ensures efficient use of the available RAM and is performed by hardware to minimize the overheads on the processor during data/voice transfers. The use of DMA ports also helps with efficient transfer of data to other peripherals.

- Full synchronous design with operation clock rate up to 160MHz.
- CPU 32KB ICache for SPI NorFlash, which can be switched to 32K SRAM when ICache is useless.
- Internal 216KB SRAM for data and program
- On-chip 8M bits serial Flash for custom defined software. Users can download program by UART.
- It is accessible for all the RAM blocks through DMA.
- Arbitrate the priority of CPU and DMA access internal RAM simultaneously.
- It is accessible for all the RAM and ROM block through CPU' data bus and program bus.

5 DMA Controller

- Support for memory-to-memory, memory-to-peripheral, and peripheral-to-memory.
- 8-channel ordinary DMA, including DMA0~7 supports for transmission in burst 8 mode. Only one of the DMA channels can transfer data at the same time.
- DMA0/DMA1/DMA2/DMA3/DMA4/DMA5/DMA6/DMA7 transmission can be triggered on the occurrence of selected events as following: memory, baseband TX & RX, modem, UART0 RX & TX, UART1 RX & TX, SPI0 RX & TX, SPI1 RX & TX, ADC, DMIC, I2S RX & TX, DAC.
- Each channel can send two interrupts to the CPU on completion of certain operational events.
- Transmission width includes 16-bit, and 32-bit, which is determined by DMA transmission type as following:
  - 8-bit: UART
  - 16-bit: ADC, DAC, I2S RX & TX, DMIC
  - 32-bit: memory, BT-baseband, BT-modem, I2S RX, DMIC

6 PMU

6.1 Features

The ATS3015P integrates a comprehensive power supply system, including the following features:

- Supports Li-Ion battery and 5V power supply
- Supports 5V power supply plugged in reset
- Supports standby current <1uA and power on button
- Integrated linear battery charger up to 300mA charging current, which supports CC/CV mode, do not support charging battery directly
- Integrated DC-DC buck converters output VD15
- Integrated linear regulators output VCC, AVCC, and AVDD
- Integrated 10-bits SAR ADC for battery voltage monitor, temperature monitor and wire-controller
- Supports DC5V insertion detection
- Supports DC5V pull out detection
- Supports communication with charger box through power line

6.2 Module Description

6.2.1 DC-DC Converter

The DC-DC converter can scales battery voltage to the required supply voltage efficiently. The DC-DC converters include several advanced features:

- Input power from BAT
- Low power consumption
- Synchronization DC-DC converter architecture
- Programmable output voltages 1.0~1.7V
- Work in Pulse Frequency Modulation (PFM) or Pulse-Width Modulation (PWM) automatically for different load current
- Support 4.7uH power inductor
- If the system is to operate from linear regulators or an external power supply, then the internal DC-DC converters are powered down automatically.

6.2.2 Linear Regulators

The ATS3015P integrates 3 linear regulators respectively generate VCC, AVCC, AVDD.
The output voltages are precisely within ±2%, providing large currents with a significantly small dropout voltage within ±5%.
Table below shows data of maximum output current.

Table 6-1 Regulators Maximum Output Current

Block Name	Input Voltage(V)	Output Voltage(V)	Output Capacitor(uF)	**Load Capacity**@ voltage drop to 95%(mA)
VCC	BAT(2.8~4.3)	3.1	1	80
AVCC	VCC(3.1)	2.95	1	10
AVDD	VD15(1.5)	1.2	1	100

6.2.3 Li-Ion Cell Charger

ATS3015P integrate charger for Li-Ion battery from a 5V source connected to the DC5V pin. The battery charger is essentially a linear regulator that has current limit and voltage limits. The charger is enable defaulted.
There is 3 phases through all the charging process: When battery voltage is below 2.8V, the charger outputs only 20mA for pre-charge. When battery voltage is between 3.0V to 4.2V, this phase is called constant current charging phase. At this phase, the charging current is constant and the voltage of battery is going up slowly. When battery voltage arrives to 4.2V, the battery voltage will be constant, and the charging current will be reduced gradually, this phase is called constant voltage phase.
One can programmatically monitor the battery voltage using the BATADC. The charger has its own voltage limiting that operates independently of the BATADC. But monitoring the battery voltage and DC5V voltage during the charge might be helpful for reporting the charge progress.
The TEMPADC can be used to monitor battery temperatures.
The SENSEADC is used to monitor the charger and diode's temperature.

7 System Control

7.1 RMU

- The RMU (Reset Management Unit) can reset all the peripherals
- The MCU can enter power-saving mode by setting the registers of RMU
- Each module has a separate reset control unit

7.2 CMU

- Support only one oscillator inputs: 24MHz
- Supply three PLLs and special clocks of all modules, the three PLLs are SPLL, Core_PLL, and Audio_PLL
- Core_PLL support spread spectrum

7.3 Timer

- Built-in a 32k oscillator
- Two Timers with IRQS using High frequency oscillator
- A watch dog which can be configured as IRQ or Reset

7.4 Exceptions and Interrupts Controller (INTC)

The ATS3015P adds additional controller to manage up to 32 interrupt sources.

Table 7-1 Interrupt Sources

Interrupt Number	Sources	Type
0	BT_BASEBAND	High Level
1	DMA	High Level
2	Watch Dog	High Level
3	TIMER0	High Level
4	TIMER1	High Level
5	SPI0	High Level
6	UART0	High Level
7	SIRQ	High Level
9	DAC_I2S TX	High Level
10	ADC	High Level
12	TWI0	High Level
14	DMIC_I2S RX	High Level
15	UART1	High Level
17	SPI1	High Level
18	TWI1	High Level
8, 11, 13, 16, 19~31	Reserved	High Level

8 Serial Interfaces

8.1 UART

ATS3015P contains two UART interfaces named UART0 and UART1. Each has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 8 Byte Transmit and Receive FIFOs while both was in 16 levels depth
- Capable of speeds up to 6Mbps to other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system

8.2 TWI

ATS3015P contains two TWI interfaces named TWI0 and TWI1. Each has the following features:

- Both master and slave functions support
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Support fifo and non_fifo mode when W/R the data
- The sequence of data or address transfer from MSB
- Only 7bit address mode is supported
- 8bit x 8 TX FIFO and 8bit x 8 RX FIFO

Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal pull-Up resistor in standard and fast mode.

8.3 SPI

ATS3015P contains two SPI interfaces named SPI0 and SPI1. SPI0 is used to connect to Nor Flash. SPI1 can be customized by customers.

- Support SPI normal mode: mode 0/1/2/3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data

9 Audio Interfaces

9.1 ADC

- Built-in mono 16-bits input sigma-delta ADC
- SNR 85dB (typ.), THD+N -81dB (typ.)
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Supports mono single-ended input analog microphone
- Supports digital microphones
- ADC and DMIC are mutually exclusive

9.2 DAC

- Built-in stereo 20-bits input sigma-delta DAC
- In differential output mode: SNR 99dB (typ.), SNR (A-Weighting) 101dB (typ.), Noise < 6uV, DR 92dB (typ.), THD+N -85dB (typ.)
- DAC supports sample rate 8k/12k/11.025k/ 16k/22.05k/24k/32k/44.1k/48k/96kHz
- Built-in stereo 20mW PA(Power Amplifier) for headphone
- The PA output supports traditional mode (non-direct drive mode) and differential mode
- The Power Amplifier drive external Power Amplifier with low noise, low distortion
- An anti-pop circuit for suppressing noise of PA when enable and disable

9.3 I2S TX

- Support I2S Transmitter(TX) with master mode
- I2S TX supports Sample Rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/88.2k/96kHz

9.4 I2S RX

- Support with master mode and slave mode
- I2S RX supports Sample Rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48kHz
- Support I2S/ left-justified/ right-justified/ TDM format, with 16/20/24 bit data width
- Support TDM 4/8 channel, with A/B mode
- Support sample rate auto detect in slave mode

10 GPIO

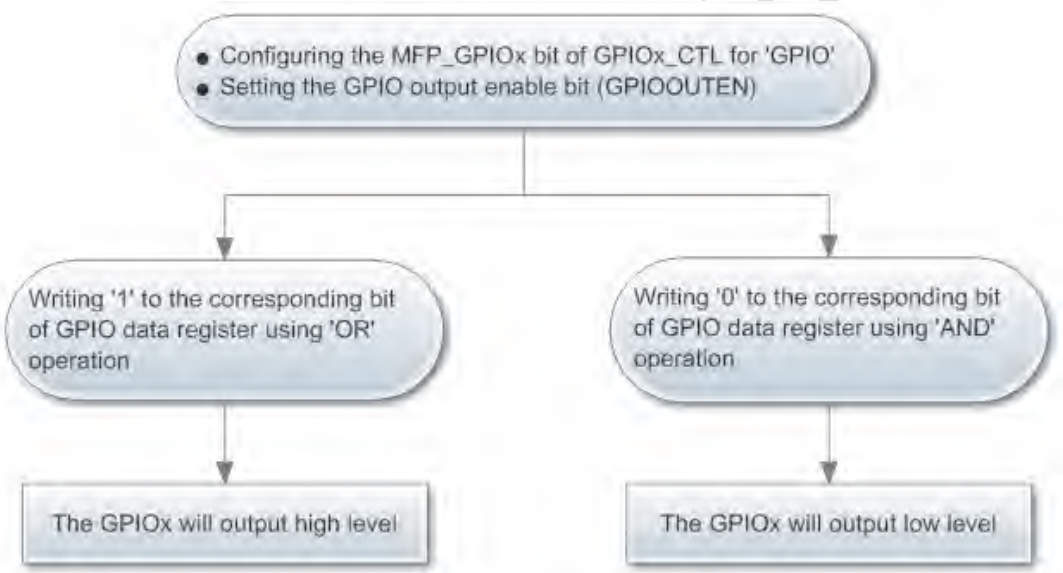
10.1 GPIO Features

GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers. All GPIOs are multiplexed with other functions to reduce the pin count.

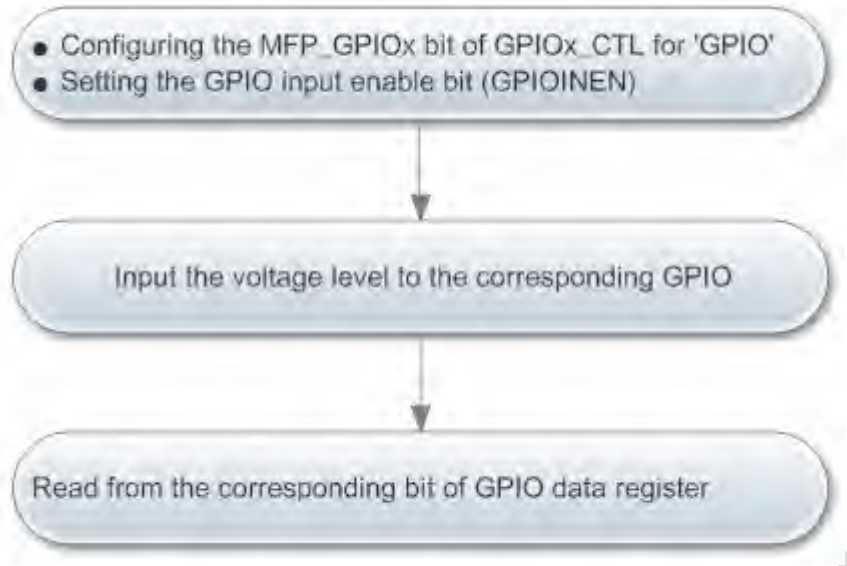
- Supports 10 GPIO
- Built-in two pull-up (100kΩ/10kΩ) and one pull-down (100kΩ) configurable resistance for the GPIO pin
- Driving strength can be adjusted which has 4 Level
- The Schmitt trigger can be configured to open or close
- Support 5 channels PWM output
- An external interruption SIRQ

10.2 GPIO Operation Manual

10.2.1 GPIO Output



10.2.2 GPIO Input



10.3 GPIO Register List

Table 10-1 GPIO Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_REGISTER	0xC00A0000	0xC00A0000

Table 10-2 GPIO Registers

Offset	Register Name	Description
0x04	GPIO0_CTL	GPIO Multiplexing Control 0
0x08	GPIO1_CTL	GPIO Multiplexing Control 1
0x0C	GPIO2_CTL	GPIO Multiplexing Control 2
0x10	GPIO3_CTL	GPIO Multiplexing Control 3
0x14	GPIO4_CTL	GPIO Multiplexing Control 4
0x18	GPIO5_CTL	GPIO Multiplexing Control 5
0x1C	GPIO6_CTL	GPIO Multiplexing Control 6
0x20	GPIO7_CTL	GPIO Multiplexing Control 7
0x24	GPIO8_CTL	GPIO Multiplexing Control 8
0x28	GPIO9_CTL	GPIO Multiplexing Control 9
0x54	GPIO_ODAT	GPIO Output Data Register
0x58	GPIO_BSR	GPIO Output Data Bit Set Register
0x5C	GPIO_BRR	GPIO Output Data Bit Reset Register
0x60	GPIO_IDAT	GPIO Input Data Register

10.4 GPIO Register Description

10.4.1 GPIO0_CTL

GPIO0 Multi-Function Control Register
Offset = 0x04

Bit(s)	Name	Description	RW	Reset

31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO0 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO0 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO0 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO0 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO0 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO0 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO0 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO0	Multi-Function of GPIO0 0: GPIO0 1: SARADC 3: UART0_TX 4: UART1_TX 5: TWI1_SDA 6: SDC_CLK Others: Reserved	R/W	0x0

10.4.2 GPIO1_CTL

GPIO1 Multi-Function Control Register
Offset = 0x08

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO1 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO1 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO1 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO1 100K PU Enable 0: Disable	R/W	0x0

		1: Enable		
6	SMIT	PAD Schmitt Enable Bit of GPIO1 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO1 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO1 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO1	Multi-Function of GPIO1 0: GPIO1 1: PWM0 2: UART0_TX 5: TWI0_SCL 6: USB_DP Others: Reserved	R/W	0x0

10.4.3 GPIO2_CTL

GPIO2 Multi-Function Control Register
Offset = 0x0C

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO2 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO2 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO2 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO2 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO2 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO2 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO2 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO2	Multi-Function of GPIO2 0: GPIO2 1: PWM1 2: UART0_RX 4: TWI0_SDA	R/W	0x0

		5: DMIC_CLK 6: USB_DM Others: Reserved		

10.4.4 GPIO3_CTL

GPIO3 Multi-Function Control Register
Offset = 0x10

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO3 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO3 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO3 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO3 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO3 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO3 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO3 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO3	Multi-Function of GPIO3 0: GPIO3 1: PWM2 2: UART0_CTS 3: I2STX_MCLK 6: UART0_TX 7: I2SRX_MCLK 8: TWI1_SCL 9: SDC_CMD Others: Reserved	R/W	0x0

10.4.5 GPIO4_CTL

GPIO4 Multi-Function Control Register
Offset = 0x14

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO4 PAD Drive Control 00: Level 1	R/W	0x2

		01: Level 2 10: Level 3 11: Level 4		
9	GPIOPDEN	GPIO4 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO4 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO4 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO4 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO4 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO4 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO4	Multi-Function of GPIO4 0: GPIO4 1: PWM3 2: UART0_RTS 3: I2STX_LRCLK 5: UART0_TX 6: UART1_RX 7: I2SRX_LRCLK 8: SDC_DAT0 Others: Reserved	R/W	0x0

10.4.6 GPIO5_CTL

GPIO5 Multi-Function Control Register
Offset = 0x18

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO5 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO5 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO5 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO5 100K PU Enable 0: Disable 1: Enable	R/W	0x0

6	SMIT	PAD Schmitt Enable Bit of GPIO5 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO5 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO5 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO5	Multi-Function of GPIO5 0: GPIO5 1: PWM4 2: I2STX_BCLK 6: UART1_CTS 7: I2SRX_BCLK 8: SPI1_CLK 9: SDC_CLK Others: Reserved	R/W	0x0

10.4.7 GPIO6_CTL

GPIO6 Multi-Function Control Register
Offset = 0x1C

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO6 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO6 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO6 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO6 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO6 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO6 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO6 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO6	Multi-Function of GPIO6 0: GPIO6 1: PWM0 2: I2STX_DOUT	R/W	0x0

		3: SIRQ 4: TEMPADC 6: UART1_RTS 7: I2SRX_DIN 8: SPI1_SS 9: SDC_CMD Others: Reserved		

10.4.8 GPIO7_CTL

GPIO7 Multi-Function Control Register
Offset = 0x20

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO7 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO7 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO7 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOPUEN	GPIO7 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt enable bit of GPIO7 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO7 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO7 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO7	Multi-Function of GPIO7 0: GPIO7 1: PWM1 4: TWI0_SCL 5: DMIC_DAT 7: SPI1_MOSI 8: SDC_DAT0 9: USB_DP Others: Reserved	R/W	0x0

10.4.9 GPIO8_CTL

GPIO8 Multi-Function Control Register
Offset = 0x24

31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO8 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO8 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO8 10K PU Enable 0: Disable 1: Enable	R/W	0x0
31:12	Reserved	Reserved	R	0x0
7	GPIOPUEN	GPIO8 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO8 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO8 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO8 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO8	Multi-Function of GPIO8 0: GPIO8 1: PWM2 4: TWI0_SDA 5: SARADC 6: DMIC_CLK 7: SPI1_MISO 8: TWI1_SCL 9: USB_DM Others: Reserved	R/W	0x0

10.4.10 GPIO9_CTL

GPIO9 Multi-Function Control Register
Offset = 0x28

Bit(s)	Name	Description	RW	Reset
31:12	Reserved	Reserved	R	0x0
11:10	PADDRV	GPIO9 PAD Drive Control 00: Level 1 01: Level 2 10: Level 3 11: Level 4	R/W	0x2
9	GPIOPDEN	GPIO9 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	10KPUEN	GPIO9 10K PU Enable 0: Disable	R/W	0x0

		1: Enable		
7	GPIOPUEN	GPIO9 100K PU Enable 0: Disable 1: Enable	R/W	0x0
6	SMIT	PAD Schmitt Enable Bit of GPIO9 0: Disable 1: Enable	R/W	0x0
5	GPIOINEN	GPIO9 Input Enable 0: Disable 1: Enable	R/W	0x0
4	GPIOOUTEN	GPIO9 Output Enable 0: Disable 1: Enable	R/W	0x0
3:0	MFP_GPIO9	Multi-Function of GPIO9 0: GPIO9 1: PWM3 2: SIRQ 3: VMIC 4: TWI0_SDA 5: DMIC_CLK 6: UART0_RX 7: TWI1_SDA Others: Reserved	R/W	0x0

10.4.11 GPIO_ODAT

GPIO Output Data Register
Offset = 0x54

Bit(s)	Name	Description	RW	Reset
31:10	Reserved	Reserved	R	0x0
9:0	GPIO_ODAT	GPIO[9:0] Output Data	R/W	0x0

10.4.12 GPIO_BSR

GPIO Output Data Bit Set Register
Offset = 0x58

Bit(s)	Name	Description	RW	Reset
31:10	Reserved	Reserved	R	0x0
9:0	GPIO_BSR	Set GPIO[9:0] Output Data bit 0: No effect 1: Set the corresponding GPIO_ODAT bit to 1, writing '1' to clear it	R/W	0x0

10.4.13 GPIO_BRR

GPIO Output Data Bit Reset Register
Offset = 0x5c

Bit(s)	Name	Description	RW	Reset
31:10	Reserved	Reserved	R	0x0
9:0	GPIO_BRR	GPIO[9:0] Output Data bit reset 0: No effect	R/W	0x0

		1: Set the corresponding GPIO_ODAT bit to 0, writing '1' to clear it		

10.4.14 GPIO_IDAT

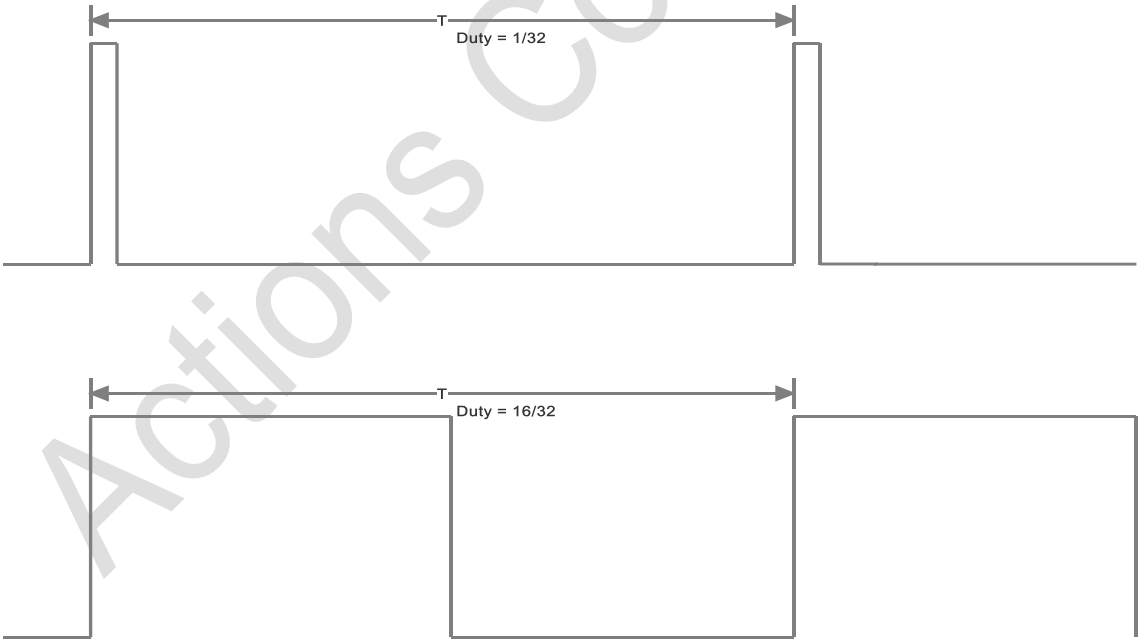
GPIO Input Data Register
Offset = 0x60

Bit(s)	Name	Description	RW	Reset
31:10	Reserved	Reserved	R	0x0
9:0	GPIO_IDAT	GPIO[9:0] Input Data	R	0x0

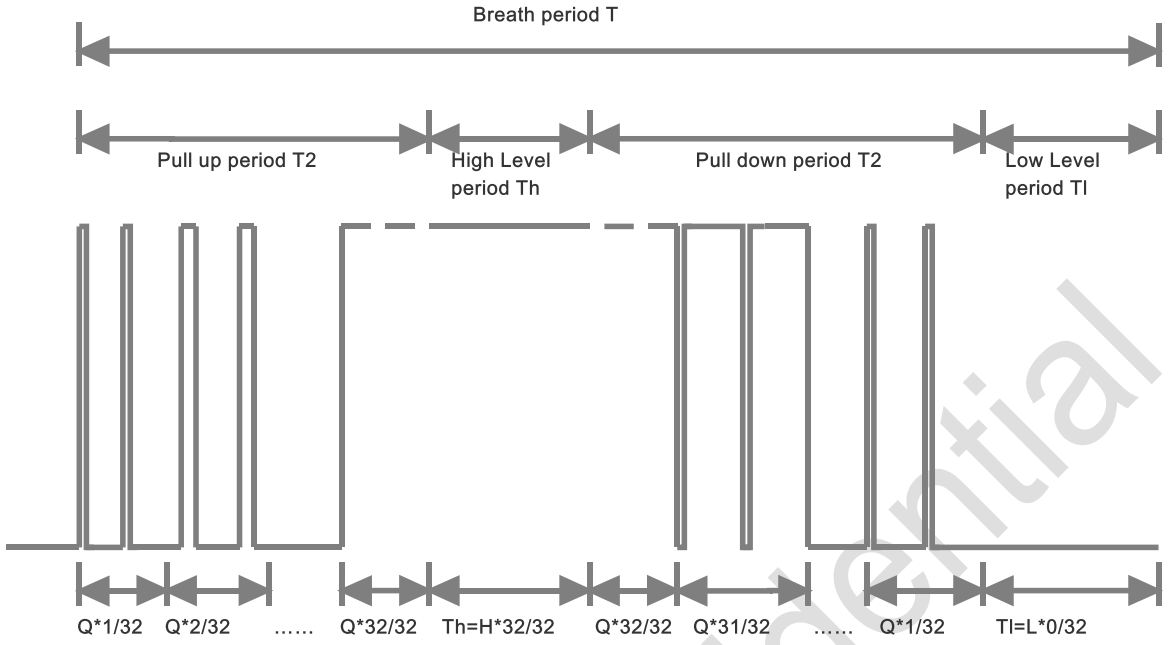
11 PWM

PWM output module is embedded in ATS3015P, in the purpose of controlling the external backlight, indicator or Bluetooth Breath Led. It supplies widely variable output frequency from 32KHz to 24MHz and 32-level duty occupancy for precise adjustment.
There are five independent PWM can be used, namely PWM0, PWM1, PWM2, PWM3, PWM4. Each PWM has two modes, namely Normal Mode and Breath Mode.

11.1 Normal Mode Timing



11.2 Breath Mode Timing



12 Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Ambient Temperature	Tamb	TBD	TBD	°C
Storage temperature	Tstg	-55	+150	°C
ESD Stress voltage	Vesd (Human body model)	4000	-	V
Supply Voltage	DC5V	-0.3	6	V
	BAT	-0.3	4.5	V
	VCC /AVCC	-0.3	3.6	V
	AVDD	-0.3	1.26	V
Input Voltage	3.1V IO	-0.3	3.6	V

Note:

1) *Even if one of the above parameters exceeds the absolute maximum ratings momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the value exceeding, which the product may be physically damaged. Use the product well within these ratings.*
2) *All voltage values are with respect to GND.*

12.2 Recommended Power Supply

Supply Voltage	Min	Typ	Max	Unit
BAT（Li）	3.2	3.8	4.35	V
DC5V	4.5	5	6	V
VCC/AVCC	2.8	3.1	3.4	V
AVDD	1.08	1.2	1.26	V

12.3 DC Characteristics

Parameter	Symbol	MIN.	MAX.	Unit	Condition
Low-level input voltage	VIL		0.6	V	3.1V GPIO pin VCC = 3.1V Tamb = -10 to 70 °C
High-level input voltage	VIH	2.4		V	
Low-level output voltage	VOL		0.6	V	
High-level output voltage	VOH	2.4		V	

12.4 Battery Charger

Parameter	Min.	Typ.	Max.	Unit
Input Voltage	BAT+0.1	5	6	V
Charge Current (CC Mode)	10	60	300	mA
Trickle Charge Current	-	20	-	mA
Trickle Charge Threshold Voltage	-	2.8	-	V
Regulated Output (Float) Voltage	3.3	4.2	4.35	V

12.5 Power Consumption

VDD = 1.1V @ 25°C, without speaker and led loading, RF TX power = +6dBm, Vbat = 3.8V

Parameter	Condition	Min.	Typ.	Max.	Unit
A2DP	ATWS, SBC bit pool = 49	-	6.2	-	mA
HFP	ATWS, Sample Rate 16KHz	-	9.2	-	mA
Sniff Mode	500ms	-	260	-	µA
Deep Sleep	Vbat = 3.8V	0.1	-	1	µA

12.6 Bluetooth Characteristics

12.6.1 Transmitter BT Classic Basic Data Rate(BDR)

Parameter	Condition	Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR	-	-	10		dBm
RF PWR Control Step	-	2	4	8	dB
20dB Bandwidth for Modulated Carrier	-	-	914	1500	KHz
Adjacent Channel Transmit	+2 MHz	-		-20	dBm
	-2 MHz	-		-20	dBm
	+3 MHz	-		-40	dBm
	-3 MHz	-		-40	dBm
Frequency Deviation	Δf1avg	140	162	175	KHz
	Δf2 99%	115	160		KHz
	Δf1avg/Δf2avg	0.8	1		
Initial Carrier Frequency Tolerance	-	-75	10	75	KHz
Frequency Drift	DH1 Packet	-25	+/-8	25	KHz
	DH3 Packet	-40	+/-8	40	KHz
	DH5 Packet	-40	+/-8	40	KHz
Frequency Drift Rate	-	-20	+/-5	20	KHz/50us
Harmonic Content	-	-	-40	-	dBm

12.6.2 Transmitter BT Classic Enhanced Data Rate(EDR)

Description		Min	Typ.	Max.	Unit
Maximum RF Transmit PWR			10		dBm
Relative Transmit PWR(EDR)		-4	-2.5	1	dB
π/4 DQPSK max carrier frequency stability|ω_0|		-10	+/-2	10	KHz
π/4 DQPSK max carrier frequency stability|ω_i|		-75	+/-5	75	KHz
π/4 DQPSK max carrier frequency stability|$\omega_0+\omega_i$|		-75	-3	75	KHz
8DPSK max carrier frequency stability |ω_0|		-10	+/-3	10	KHz
8DPSK max carrier frequency stability |ω_i|		-75	+/-5	75	KHz
8DPSK max carrier frequency stability|$\omega_0+\omega_i$|		-75	+/-5	75	KHz
π/4 DQPSK Modulation Accuracy	RMS DEVM		6	20	%
	99% DEVM	99	100		%
	Peak DEVM		15	35	%
In-band spurious emissions	F >F0 + 3MHz			-40	dBm
	F < F0 - 3MHz			-40	dBm
	F = F0 + 3MHz			-40	dBm
	F = F0 - 3MHz			-40	dBm
	F = F0 + 2MHz			-20	dBm
	F = F0 - 2MHz			-20	dBm
	F = F0 + 1MHz			-26	dBm
	F = F0 - 1MHz			-26	dBm
EDR Differential Phase Encoding		99	100		%

12.6.3 Transmitter Bluetooth Low Energy(BLE) 1Mbps

Description		Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR			10		dBm
In-band emissions	+2 MHz		-45	-20	dBm
	-2 MHz		-46	-20	dBm
	+3 MHz		-48	-30	dBm
	-3 MHz		-47	-30	dBm
Modulation Characteristics	Δf1avg	225	248	275	KHz
	Δf2 99%	185	240		KHz
	Δf1avg/Δf2avg	0.8	1		
Carrier Frequency Offset		-150	+/-10	150	KHz
Frequency Drift		-50	+/-5	50	KHz

12.6.4 Transmitter Bluetooth Low Energy(BLE) 2Mbps

Description		Min.	Typ.	Max.	Unit
Maximum RF Transmit PWR			10		dBm
Adjacent Channel Transmit	+2 MHz		-54	-20	dBm
	-2 MHz		-54	-20	dBm
	+3 MHz		-58	-30	dBm
	-3 MHz		-58	-30	dBm
Frequency Deviation	Δf1avg	450	506	550	KHz
	Δf2 99%	370	420		KHz
	Δf1avg/Δf2avg	0.8	0.85		
Carrier Frequency Offset		-150	+/-10	150	KHz
Frequency Drift		-50	+/-5	50	KHz
Frequency Drift Rate		-20	-3	20	KHz/50us

12.6.5 Receiver BT Classic Basic Data Rate(BDR)

Description		Min.	Typ.	Max.	Unit
Sensitivity			-95		dBm
Maximum Input PWR at 0.1% BER		-20			dBm
Co-Channel Interface		-	<11		dB
Adjacent Channel Selectivity C/I	$F = F_0 + 1MHz$	-	<0		dB
	$F = F_0 - 1MHz$	-	<0		dB
	$F = F_0 + 2MHz$	-	<-30		dB
	$F = F_0 - 2MHz$	-	<-30		dB
	$F = F_0 + 3MHz$	-	<-40		dB
	$F = F_{image}$	-	<-9		dB

12.6.6 Receiver BT Classic Enhanced Data Rate(EDR)

Description		Min.	Typ.	Max.	Unit
Sensitivity at 0.1% BER	π/4 DQPSK		-94	-	dBm
	8DPSK		-88	-	dBm
Maximum Input PWR at 0.1% BER	π/4 DQPSK	-20			dBm
	8DPSK	-20			dB
C0-Channel Interference	π/4 DQPSK	-	<13		dB
	8DPSK	-	<21		dB

12.6.7 Receiver Bluetooth Low Energy(BLE) 1Mbps

Description		Min.	Typ.	Max.	Unit
Sensitivity LE 1M			-99		dBm
Maximum Input PWR at 0.1% BER		-10			dBm
C/I	Co-channel		<21		dB
	Adjacent 1Mhz		<15		dB
	Adjacent 2MHz		<-17		dB
	Adjacent >=3Mhz		<-27		dB
	Image interference		<-9		dB
	Image+/-1Mhz		<-15		dB
Blocking	30Mhz~2000Mhz	-30			dBm
	2000Mhz~2400MHz	-35			dBm
	2500MHz~3000MHz	-35			dBm
	3000MHz~12.75Ghz	-30			dBm

12.6.8 Receiver Bluetooth Low Energy(BLE) 2Mbps

Description		Min.	Typ.	Max.	Unit
Sensitivity LE 2M			-96		dBm
Maximum Input PWR at 0.1% BER		-10			dBm
C/I	Co-channel		<21		dB
	Adjacent 1Mhz		<15		dB
	Adjacent 2MHz		<-17		dB
	Adjacent >=3Mhz		<-27		dB
	Image interference		<-9		dB
	Image+/-2Mhz		<-15		dB
Blocking	30Mhz~2000Mhz	-30			dBm
	2000Mhz~2400MHz	-35			dBm
	2500MHz~3000MHz	-35			dBm
	3000MHz~12.75Ghz	-30			dBm

12.7 Audio ADC

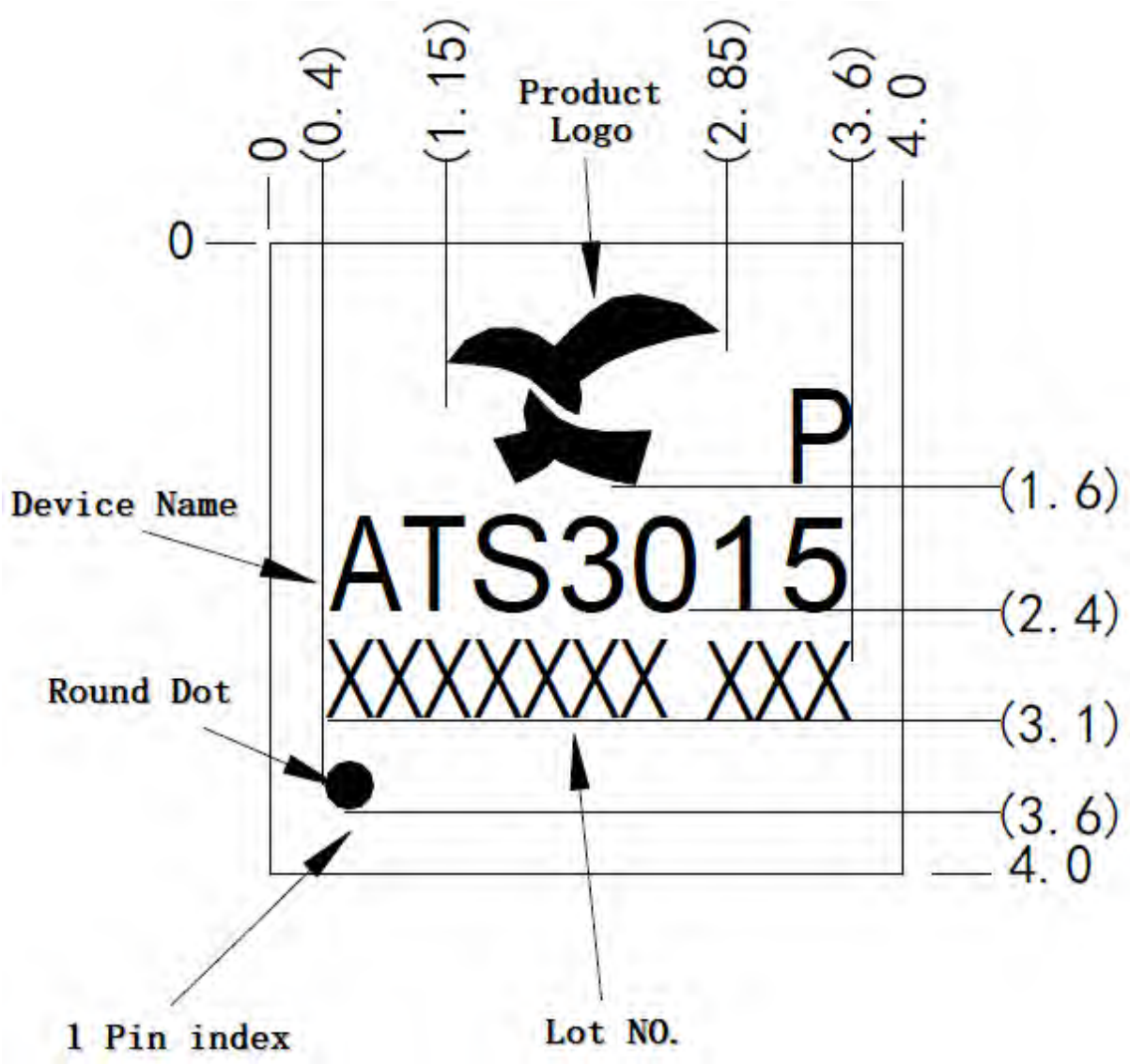
Pre-Amplifier						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Full Scale Input Voltage	THD+N < 1% (MIC OP = 18dB)		-	-	144	mVpp
Analogue gain	MIC OP	Single Ended	9	-	36	dB
Analogue to Digital Converter						
Resolution	-		-	-	16	Bits
Input Sample Rate	-		8	-	48	kHz
SNR	fin = 1kHz@144mVpp B/W = 22Hz~8kHz, Fs=16kHz		-	85	-	dB
Dynamic Range	fin = 1kHz@1.44mVpp B/W = 22Hz~8kHz, Fs = 16kHz		-	85	-	dB
THD+N	fin = 1kHz(input=117mVpp) B/W = 22Hz~8kHz, Fs=16kHz		-	-81	-	dB
Digital gain	-		0	-	18	dB

12.8 Stereo DAC

Digital to Analogue Converter						
Parameter	**Conditions**		**Min**	**Typ**	**Max**	**Unit**
Resolution	-		-	-	20	Bits
Output Sample Rate	-		8	-	96	kHz
SNR	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	99	-	dB
		A-Weighting	-	101	-	dB
	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω Enable noise mute(1)	-	-	108	-	dB
		A-Weighting	-	110	-	dB
Dynamic Range	fin = 1kHz@-40dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	92	-	dB
		A-Weighting	-	94	-	dB
THD+N	fin = 1kHz@0dBFS input B/W = 22Hz~22kHz Fs=48kHz,Load=16Ω	-	-	-85	-	dB
Digital gain	-		<-60	-	30	dB
Stereo crosstalk	fin = 1kHz@0dBFS input	Differential output	-	-114	-	dB
PWR Amplifier						
Max Amplitude/PWR	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Single Ended Output	-	-	275	mVrms
			-	-	5	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=16Ω	Full Differential Output	-	-	534	mVrms
			-	-	20	mW
	fin = 1kHz@0dBFS input Fs=48kHz,Load=10KΩ	Full Differential Output	-	-	1.6	Vpp

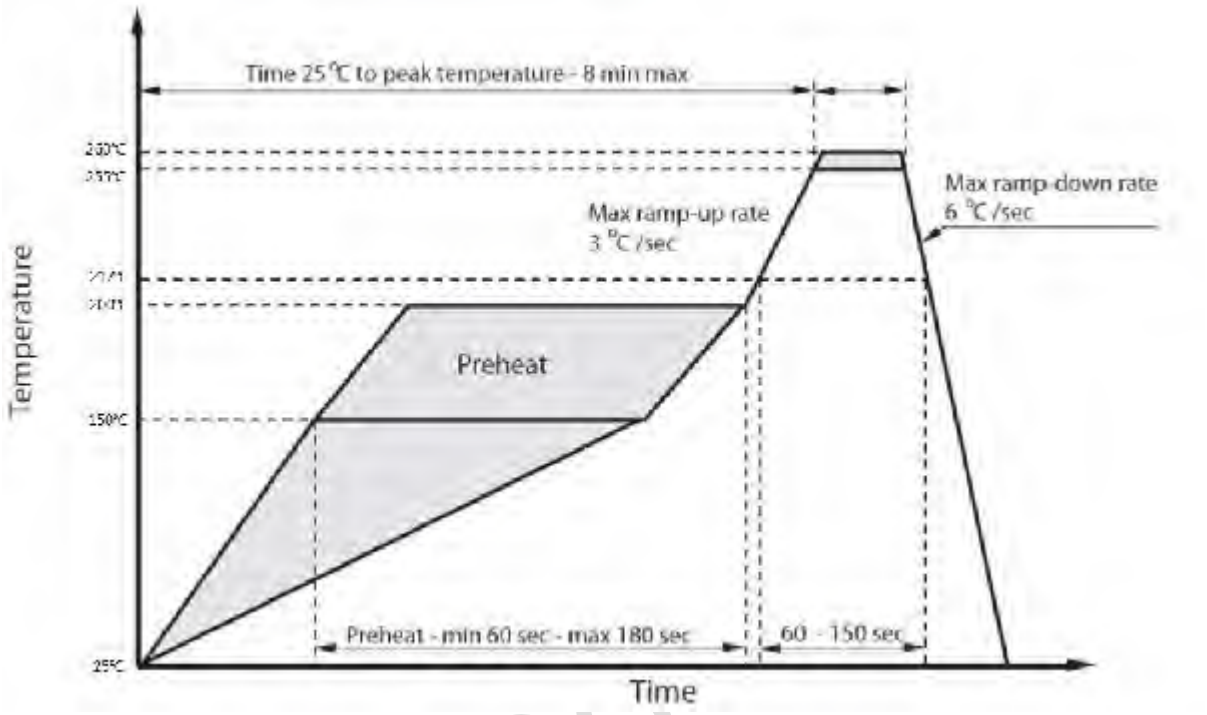
Note:
(1) If the data path is idle, noise mute function should be enabled to ensure the best noise performance.

13 Device Marking of the Chipset



14 Reflow Solder Information

The ATS3015P is constructed with all RoHS compliant material and should be reflowed accordingly. This chip is Moisture Sensitivity Level MSL3 and must be stored and handled accordingly.



Acronyms and Abbreviations

Abbreviations	Descriptions
AEC	acoustic echo cancellers
ADC	Analog to Digital Converter
AGC	Auto Gain Control
CMU	Clock Management Unit
DAC	Digital to Analog Converter
DMA	Direct Memory Access
GPIO	General Purpose Input Output
HOSC	High Frequency OSC (24MHz)
INTC	Interrupt Controller
IRQ	Interrupt Request
SARADC	Successive Approximation Register Analog to Digital Converter
MIC	Microphone
MFP	Multiple Function PAD
NMI	Nonmaskable Interrupt
OSC	Oscillator
PA	Power Amplifier
SNR	Signal to Noise Ratio
DR	Dynamic Range
PMU	Power Management Unit
PWM	Pulse Width Modulation
RMU	Reset Management Unit
SIE	Serial Interface Engine
ATWS	Actions Ture Wireless Stereo

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