		1: TX IRQ Pending.		
2	SPI_RIRQ_PD	SPI1 RX IRQ Pending, Writing '1' to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	SPI_READY	SPI1 Ready (AHB Interface Only, please reference operation manual) 0: not ready 1: ready	R	0x1
0	SPI_BUSY	SPI1 master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

10.5.3.3 SPI1_TXDAT

SPI1 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:0	SPI1_TXDAT	SPI1 TX FIFO, 32bitx16 levels When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

10.5.3.4 SPI1_RXDAT

SPI1 Receive FIFO Data Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	SPI1_RXDAT	SPI RX FIFO, When SPI1_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI1_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx16 levels	R	0x0

10.5.3.5 SPI1_BC

SPI1 Bytes Count Register, this register is used for setting SPI1 bytes counter bits in the SPI read mode only.
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received, only use in master mode	R	0x0
15:0	SPI1_BC	Bytes Counter [15: 0]	R/W	0x0

10.6 SPI2

10.6.1 Features

- Support SPI normal mode: mode 0/1/2/3

- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data
- Support 16 level delay chain, 1ns/step
- Support slave mode
- Support 100MHz spi_clk as highest speed

10.6.2 SPI2 Register List

Table 10-13 SPI2 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI2	0xC01B0000	0xC01B0000

Table 10-14 SPI2 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI2_CTL	SPI2 Control Register
0x0004	SPI2_STA	SPI2 Status Register
0x0008	SPI2_TXDAT	SPI2 Transmit FIFO Data Register
0x000C	SPI2_RXDAT	SPI2 Receive FIFO Data Register
0x0010	SPI2_BC	SPI2 Byte Counter Register

10.6.3 SPI2 Register Description

10.6.3.1 SPI2_CTL

SPI2 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27	-	Reserved	R/W	0x0
26	RX_WRITE_SEL	SPI2 Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
25	DMS	DMA transmit mode select 0: burst8 mode 1: single mode	R/W	0x0
24	TXCEB	TX Convert Endian bit， only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476	R/W	0x0

		When in 8 bit mode, this bit have no effect		
23	RXCEB	RX Convert Endian bit， only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0
20	RILS	RX IRQ Level select 0: RX FIFO not empty, generate IRQ 1: RX FIFO at least 8 level data, generate IRQ Note: this bit have no effect when SPI_RIRQ_EN is disable, SPI2_CTL[8].	R/W	0x0
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: 1 unit delay 0010: 2 units delay 0011: 3 units delay 0100: 4 units delay 0101: 5 units delay 0110: 6 units delay 0111: 7 units delay 1000: 8 units delay 1001: 9 units delay 1010: 10 units delay 1011: 11 units delay 1100: 12 units delay 1101: 13 units delay 1110: 14 units delay 1111: 15 units delay	R/W	0x0
15:10	-	Reserved	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO at least 8 level empty 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, this trigger of SPI RX IRQ controlled by SPI2_CTL[20]. 0: disable 1: enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full; When DMA remain counter < 8, trigger DRQ until all data received completely 0: disable	R/W	0x0

		1: enable		
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

10.6.3.2 SPI2_STA

SPI2 Status Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
10	-	Reserved	R	0x0
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
7	SPI_RXFU	SPI2 RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI2 RX FIFO Empty 0: not empty 1: empty	R	0x1
5	SPI_TXFU	SPI2 TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI2 TX FIFO Empty 0: not empty 1: empty	R	0x1
3	SPI_TIRQ_PD	SPI2 TX IRQ Pending, Writing '1' to this bit will clear it. 0: No TX IRQ Pending	R/W	0x0

		1: TX IRQ Pending.		
2	SPI_RIRQ_PD	SPI2 RX IRQ Pending, Writing '1' to this bit will clear it. 0: No RX IRQ Pending 1: RX IRQ Pending.	R/W	0x0
1	-	Reserved	R	x
0	SPI_BUSY	SPI2 master busy status bit. 0: SPI idle status 1: SPI busy status (Clock is transmiting or Rx Remain Counter doesn't reduced to zero)	R	0x0

10.6.3.3 SPI2_TXDAT

SPI2 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:0	SPI2_TXDAT	SPI2 TX FIFO, 32bitx16 levels When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid. Be read as zero.	W	0x0

10.6.3.4 SPI2_RXDAT

SPI2 Receive FIFO Data Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	SPI2_RXDAT	SPI RX FIFO, When SPI2_CTL[30] select 8bit width, bit[7:0] is valid. 8bitx64levels When SPI2_CTL[30] select 32bit width, bit[31:0] is valid. 32bitx16 levels	R	0x0

10.6.3.5 SPI2_BC

SPI2 Bytes Count Register, this register is used for setting SPI2 bytes counter bits in the SPI read mode only.
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	REMAIN_CNT	Indicate how many bytes need to be received, only use in master mode	R	0x0
15:0	SPI2_BC	Bytes Counter [15:0]	R/W	0x0

10.7 PWM

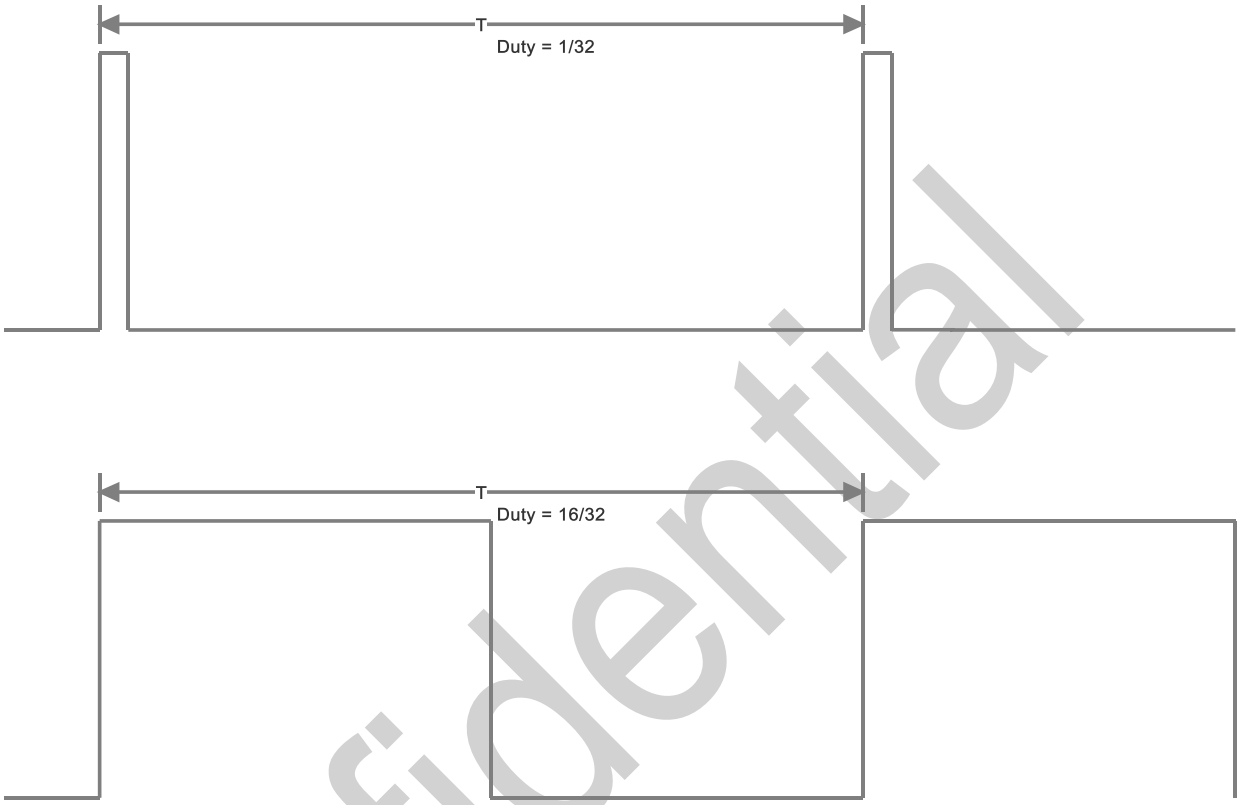
10.7.1 Features

- Independent of 9 PWM
- The frequency of PWM comes from the division of 32KHz/HOSC/CK64M
- Support normal mode and breath mode
  - Normal mode can output 256 kinds of duty

- Breath mode supports breathing lights with various flicker frequencies

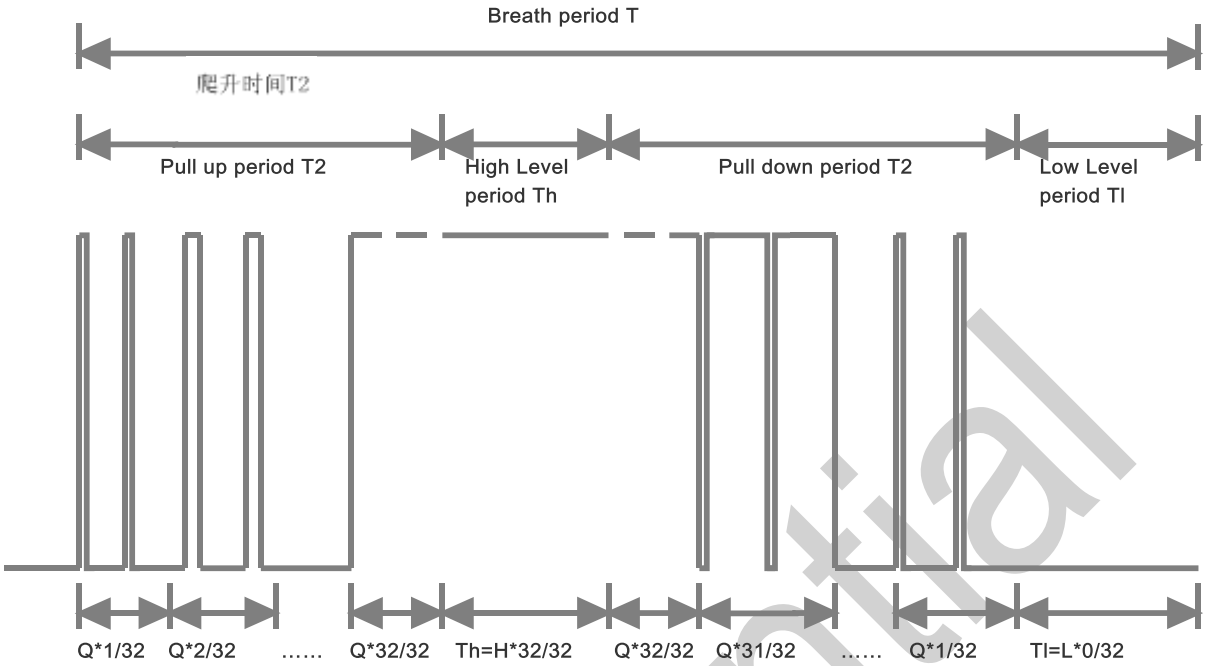
10.7.2 Module Description

10.7.2.1 Normal Mode Timing



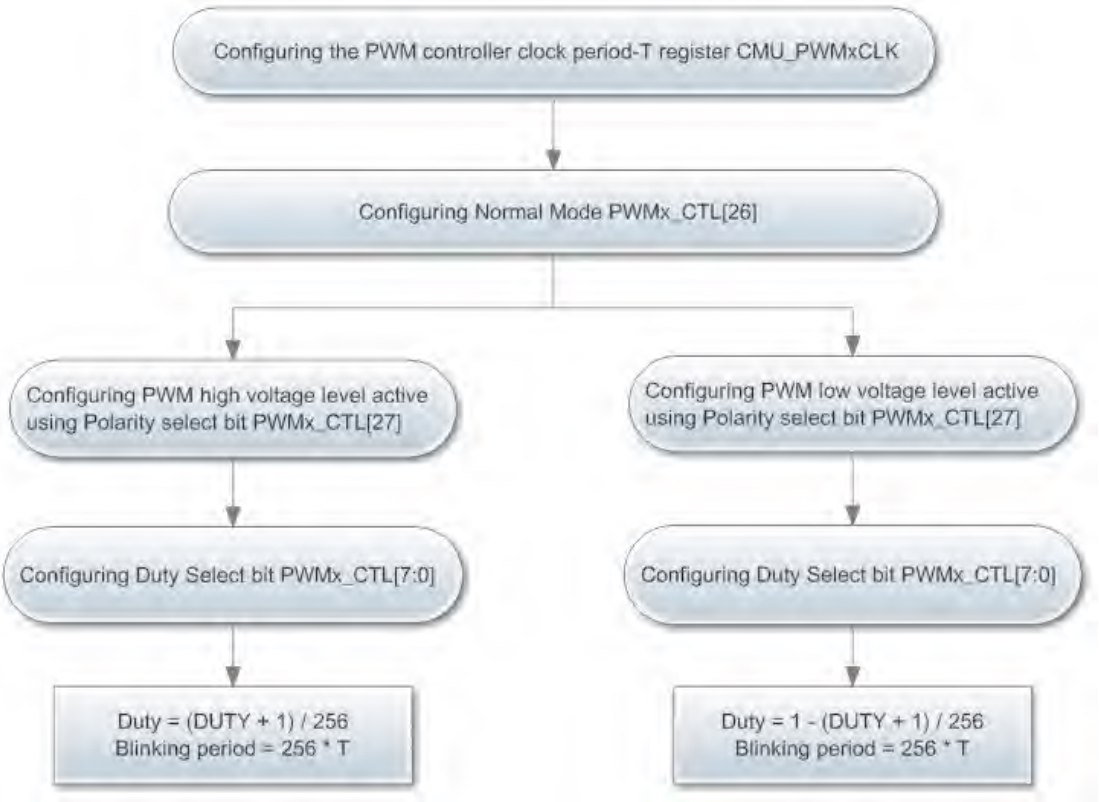
PWM can be used as backlights enable signal of LCD. The brightness of the backlights is decided by the duty cycle of PWM.

10.7.2.2 Breath Mode Timing



The breath mode of PWM can be used for driver of breathing light. For example, if PWM CLK from CMU is f=1/t and we need the time of pull up or pull down to be T2=Q*32*32t=0.5s, and the time of high level Th=H*32T=0.5s and the time of low level Tl=L*32t=2s, when we set Q=2, the f should be 4096 and H is 64, L is 256.

10.7.3 Operation Manual



For example, if Duty =50% and the Blinking period is two seconds, T=2/256, the Frequency of the PWM controller clock is 1/T=128Hz, So CMU_PWMxCLK can be configured as 0xF9, PWMx_CTL can be configured as 0x0800007F.

10.7.4 PWM Register List

Table 10-15 PWM Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
PWM	0xC0180000	0xC0180000

Table 10-16 PWM Registers Offset Address

Offset	Register Name	Description
0x0000	PWM0_CTL	PWM0 Output Control
0x0004	PWM1_CTL	PWM1 Output Control
0x0008	PWM2_CTL	PWM2 Output Control
0x000C	PWM3_CTL	PWM3 Output Control
0x0010	PWM4_CTL	PWM4 Output Control
0x0014	PWM5_CTL	PWM5 Output Control
0x0018	PWM6_CTL	PWM6 Output Control
0x001C	PWM7_CTL	PWM7 Output Control
0x0020	PWM8_CTL	PWM8 Output Control

10.7.5 PWM Register Description

10.7.5.1 PWM0_CTL

PWM0 Output Control Register
Offset=0x00

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32: Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256	R/W	0x0

		Only Active in Normal Mode		

10.7.5.2 PWM1_CTL

PWM1 Output Control Register
Offset=0x04

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.3 PWM2_CTL

PWM2 Output Control Register
Offset=0x08

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t	R/W	0x0

		t is the period of CMU_PWM		
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.4 PWM3_CTL

PWM3 Output Control Register
Offset=0x0C

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.5 PWM4_CTL

PWM4 Output Control Register
Offset=0x10

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode	R/W	0x0

		1: Breath Mode		
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.6 PWM5_CTL

PWM5 Output Control Register
Offset=0x14

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.7 PWM6_CTL

PWM6 Output Control Register
Offset=0x18

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0

26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.8 PWM7_CTL

PWM7 Output Control Register
Offset=0x1C

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable 0: Disable 1: Enable	R/W	0x0
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

10.7.5.9 PWM8_CTL

PWM8 Output Control Register
Offset=0x20

Bits	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	PWM_EN	PWM Enable	R/W	0x0

		0: Disable 1: Enable		
27	POL_SEL	Polarity select 0:PWM low voltage level active 1:PWM high voltage level active Only Active in Normal Mode	R/W	0x0
26	MODE_SEL	Mode Select: 0: Normal Mode 1: Breath Mode	R/W	0x0
25:24	Q	Time of Every Duty =1/32 …32/32 Climbing and descending time T2=(Q+1)*32*32t t is the period of CMU_PWM	R/W	0x0
23:16	H	Time of Duty =32/32 High Level Time = H*32t t is the period of CMU_PWM	R/W	0x0
15:8	L	Time of Duty =0/32 Low Level Time = L*32t t is the period of CMU_PWM	R/W	0x0
7:0	DUTY	Duty Select T Active = (Duty+1)/256 Only Active in Normal Mode	R/W	0x0

11 Audio Interface

11.1 DAC

- Build in stereo 24 bit input sigma-delta DAC, SNR>98dB, SNR (A-WEIGHTING)>101dB, THD<-87dB
- DAC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48/96kHz
- Support digital volume of 256 steps with zero cross detection
- Build in stereo 20mW PA (Power Amplifier) for headphone. PA output supports traditional mode and direct drive mode(for earphone)
- An anti-pop circuit for suppressing noise of PA when enable and disable
- Support differential audio output for speaker PA

11.2 ADC

- Build in stereo 24 bit input sigma-delta ADCs, SNR>96dB, SNR (A-WEIGHTING)>98dB, THD<-85dB
- ADC supports sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1/48/96kHz
- A digital high-pass filter can be used to remove dc offsets when ADC use
- Supports single-ended input analog microphones and full difference input microphone
- Supports Digital microphones

11.3 I2S

11.3.1 Features

- Support 3 I2S module: I2SRX0, I2SRX1, and I2STX
- I2SRX0 and I2SRX1 support I2S receiver(RX) with master mode and slave mode
- I2STX support I2S transmission(TX) with master mode and slave mode
- I2S support sample rate 8k/12k/11.025k/16k/22.05k/24k/32k/44.1k/48k/96k/192kHz

- I2S support 3 transmission modes: left-justified format, right-justified format, and I2S format

11.3.2 I2SRX0 Register List

Table 11-1 I2SRX0 Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2SRX0_Register	0xC0052100	0xC0052100

Table 11-2 I2SRX0 Controller Registers

Offset	Register Name	Description
0x0000	I2SRX0_CTL	I2SRX0 Control Register
0x0010	I2SRX0_SRDCTL	I2SRX0 sample rate detect control register
0x0014	I2SRX0_SRDSTA	I2SRX0 sample rate detect status register

11.3.3 I2SRX0 Register Description

11.3.3.1 I2SRX0_CTL

I2SRX0 Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	RX0_RX1_5W_EN	I2S RX0 and I2S RX1 in 5w mode 0 : disable 1 : enable RX1 would share the clock with RX0, when this bit set to '1', and should not set RX1_EN in this case. Master mode used only.	R/W	0x0
11:8	-	Reserved	R	0x0
7	RXMODE	I2SRX0 mode select 0: I2S Master mode 1: I2S Slave mode	R/W	0x0
6	RX_SMCLK	MCLK source when in slave mode 0: from internal module 1: from extern input by pad of MCLK Note: if there was no MCLK supply by master, this bit should be set to '1'.	R/W	0x1
5:4	RXWIDTH	Effective width 00: datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	RXBCLKSET	Rate of BCLK with LRCLK 0x0: 64*FS 0x1: 32*FS	R/W	0x0
2:1	RXMODELSEL	I2S transfer format select 00: i2s model 01: left-justified 10: right-justified 11: reserved	R/W	0x0

		Note: in case of 32FS, Lj format should not be configured.		
0	RXEN	I2SRX0 Enable 0: Disable 1: Enable	R/W	0x0

11.3.3.2 I2SRX0_SRDCTL

I2SRX0 sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the RX input as 0. 1: mute 0: not mute Mute would continue until SRC_PD was clear.	R/W	0x0
11:9	-	reserved	R/W	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0: disable 1: enable If sample rate detection module timeout, or detected sample rate changing or detected channel width changing, if would cause interrupt.	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0: 2 LRCLK cycle 1: 4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable: 0: disable 1: enable	R/W	0x0

11.3.3.3 I2SRX0_SRDSTA

I2SRX0 sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0

24:12	CNT	CNT of LRCLK which sampling by SRC_CLK CNT= Freq_ SRC_CLK / LRCLK It would clear when module was enabling at first time.	R	0x0
11	TO_PD	sample rate detect result timeout interrupt pending 0: no irq 1: irq Write '1' to clean this bit. CNT overflow (0x9c00) would cause this irq.	R/W	0x0
10	SRC_PD	sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
7:2	-	Reserved	R	0x0
1:0	WL	Channel word length(the rate of BCLK to LRCLK)： 00: 16bit (32 rate) 01: 32bit (64 rate) 1x: others	R	0x0

11.3.4 I2SRX1 Register List

Table 11-3 I2SRX1 Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2SRX1_Register	0xC0052200	0xC0052200

Table 11-4 I2SRX1 Controller Registers

Offset	Register Name	Description
0x0000	I2SRX1_CTL	I2SRX1 Control Register
0x0004	I2SRX1_FIFOCTL	I2SRX1 FIFO control register
0x0008	I2SRX1_FIFOSTAT	I2SRX1 FIFO status register
0x000C	I2SRX1_DAT	I2SRX1 FIFO data register
0x0010	I2SRX1_SRDCTL	I2SRX1 sample rate detect control register
0x0014	I2SRX1_SRDSTA	I2SRX1 sample rate detect status register

11.3.5 I2SRX1 Register Description

11.3.5.1 I2SRX1_CTL

I2SRX1 Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RXMODE	I2SRX1 mode select	R/W	0x0

		0: I2S Master mode 1: I2S Slave mode		
6	RX_SMCLK	MCLK source when in slave mode 0: from internal module 1: from extern input by pad of MCLK I2S slave mode used only. Note: if there was no MCLK supply by master, this bit should be set to '1'.	R/W	0x1
5:4	RXWIDTH	Effective width 00: datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	RXBCLKSET	Rate of BCLK with LRCLK 0x0:64*FS 0x1:32*FS	R/W	0x0
2:1	RXMODELSEL	I2S transfer format select 0 0:I2S model 01: left-justified 10: right-justified 11: reserved Note: in case of 32FS, Lj format should not be configured.	R/W	0x0
0	RXEN	I2SRX1 Enable 0: Disable 1: Enable	R/W	0x0

11.3.5.2 I2SRX1_FIFOCTL

I2SRX1 FIFO Control Register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RX1FIFO_DMAWIDTH	I2SRX1FIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . I2SRX1FIFO doesn't support 8bit and 64bit DMA data width.	R/W	0x0
6	-	Reserved	R	0x0
5:4	RXFOS	RX FIFO Output Select 0x00: CPU 0x01: DMA 0x02: Reserved 0x03: DSP	R/W	0x0
3	RXFIS	RX FIFO Input Select 0x0: I2SRX1 0x1: SPDIFRX	R/W	0x0
2	RXFFIE	RX FIFO Half Full IRQ Enable 0: Disable 1: Enable	R/W	0x0

1	RXFFDE	RX FIFO Half Full DRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
0	RXFRT	RX FIFO Reset 0x0: Reset FIFO 0x1: Enable FIFO	R/W	0x0

11.3.5.3 I2SRX1_FIFOSTAT

RX1 FIFO State Register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	RXFEF	RX FIFO Empty Flag 0x0: Not Empty 0x1: Empty	R	0x1
6	RXFIP	RX FIFO Half Full IRQ Pending Bit 0x0: No IRQ 0x1: IRQ Writing '1' to the bit is clear it.	R/W	0x0
5	-	Reserved	R	0x0
4:0	RXFS	RX FIFO Status These 5 bits shows how many sample pairs fifo filled. For example, when read as 6, means DSP can read 12 samples from fifo. If no I2SRX1_CLK, register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

11.3.5.4 I2SRX1_DAT

I2S1 RX FIFO DAT
Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:8	RXDAT	RX Data FIFO is 24bit x 32 levels.	R	x
7:0	-	Reserved	R	0x0

11.3.5.5 I2SRX1_SRDCTL

I2SRX1 sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the RX input as 0. 1:mute 0:not mute	R/W	0x0

11:9	-	Reserved	R/W	0x0
8	SRD_IE	sample rate detect result change interrupt enable 0:disable 1:enable	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0:2 LRCLK cycle 1:4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable 0: disable 1: enable	R/W	0x0

11.3.5.6 I2SRX1_SRDSTA

I2SRX1 sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRC_CLK CNT= Freq_ SRC_CLK / LRCLK It would clear when module was enabling at first time.	R	0x0
11	TO_PD	Sample rate detect result timeout interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit. CNT overflow (0x9c00) would cause this irq.	R/W	0x0
10	SRC_PD	Sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	Sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write ‘1’ to clean this bit.	R/W	0x0

7:2	-	Reserved	R	0x0
1:0	WL	Channel word length(the rate of BCLK to LRCLK)： 00: 16bit(32 rate) 01: 32bit (64 rate) 1x: others	R	0x0

11.3.6 I2STX Register List

Table 11-5 I2STX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
I2STX_Register	0xC0052000	0xC0052000

Table 11-6 I2STX Controller Registers

Offset	Register Name	Description
0x0000	I2STX_CTL	I2STX Control Register
0x0004	I2STX_FIFOCTL	I2STX FIFO control register
0x0008	I2STX_FIFOSTAT	I2STX FIFO status register
0x000C	I2STX_DAT	I2STX FIFO data register
0x0010	I2STX_SRDCTL	I2STX sample rate detect control register
0x0014	I2STX_SRDSTA	I2STX sample rate detect status register
0x0020	I2STX_FIFO_CNT	I2STX FIFO Sample Counter register

11.3.7 I2STX Register Description

11.3.7.1 I2STX_CTL

I2STX Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	MULT_DEVICE	Multi device simultaneous startup selection 0x0: Disable 0x1: I2STX with SPDIFTX	R/W	0x0
15:14	-	Reserved	R	0x0
13	I2SRX1_5W_EN	I2STX & I2SRX1 5wire enable 0:disable 1:enable RX1 would share the clock with TX, when this bit set to '1', and should not set RX1_EN in this case. Master mode used only.	R/W	0x0
12	I2SRX0_5W_EN	I2STX & I2SRX0 5wire enable 0:disable 1:enable RX0 would share the clock with TX, when this bit set to '1', and should not set RX0_EN in this case. Master mode used only.	R/W	0x0
11:10	-	Reserved	R	0x0
9	LPEN1	I2STX and I2SRX1 loopback enable 0：disable 1：enable	R/W	0x0

		When enable, I2STX send CLOCK and data to I2SRX1		
8	LPEN0	I2STX and I2SRX0 loopback enable 0 : disable 1 : enable When enable, I2STX send CLOCK and data to I2SRX0	R/W	0x0
7	TXMODE	I2STX mode select 0: Master mode 1: Slave mode	R/W	0x0
6	TX_SMCLK	MCLK(256FS) source when in slave mode 0:from internal module 1:from extern input by pad of Mclk I2S slave mode used only. Note: if there was no mclk supply by master, this bit should be set to '1'.	R/W	0x1
5:4	TXWIDTH	Effective width 00:datas are 16 bit effective 01: datas are 20 bit effective 10: datas are 24 bit effective 11: reserved	R/W	0x2
3	TXBCLKSET	Rate of BCLK with LRCLK 0x0:64*FS 0x1:32*FS	R/W	0x0
2:1	TXMODELSEL	I2S transfer format select 00 : I2S format 01 : left-justified format 10 : right-justified format 11 : reserved Note: in case of 32FS, Lj format should not be configured.	R/W	0x0
0	TXEN	I2STX Enable 0: Disable 1: Enable	R/W	0x0

11.3.7.2 I2STX_FIFOCTL

I2STX FIFO control register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	TXFIFO_DMAWIDTH	I2STXFIFO DMA transfer width configured 0 : 32bit 1 : 16bit Match width DMA width which configured at register DMAx_CTL[14:13] . I2STXFIFO doesn't to support 8bit and 64bit DMA data width.	R/W	0x0
6	ASRC_SEL	I2STX FIFO Input select when FIFO_IN_SEL select ASRC OUT 0x0 : ASRC_OUT0 0x1 : ASRC_OUT1 Only use in FIFO_IN_SEL=2b'10	R/W	0x0

5:4	FIFO_IN_SEL	I2STX_FIFO Input Select 0x00: CPU 0x01: DMA 0x02: ASRC OUT 0x03: DSP	R/W	0x0
3	FIFO_SEL	I2STX&SPDIFTX module FIFO select 0 : DAC FIFO0/1 1 : I2STX FIFO	R/W	0x0
2	FIFO_IEN	I2STX_FIFO Half Empty IRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
1	FIFO_DEN	I2STX_FIFO Half Empty DRQ Enable 0x0: Disable 0x1: Enable	R/W	0x0
0	FIFO_RST	I2STX_FIFO Reset 0x0: Reset FIFO 0x1: Enable FIFO	R/W	0x0

11.3.7.3 I2STX_FIFOSTAT

I2STX FIFO status register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	IP	I2STX_FIFO Half Empty IRQ Pending Bit 0x0: No IRQ 0x1: IRQ Writing '1' to the bit is clear it.	R/W	0x0
6	TFFU	I2STX_FIFO Full Flag 0x0: Not Full 0x1: Full	R	0x0
5	-	Reserved	R	0x0
4:0	STA	I2STX_FIFO Status Indicate how many fifo level can be written into fifo. If no I2STX_CLK register would display zero. If fill (n*2+1) level fifo, register would display n level.	R	0x0

11.3.7.4 I2STX_DAT

I2STX FIFO data register
Offset = 0x0c

Bit (s)	Name	Description	Access	Reset
31:8	DAT	I2STX_FIFO Data FIFO is 24bit x 32 levels.	W	x
7:0	-	Reserved	R	0x0

11.3.7.5 I2STX_SRDCTL

I2STX sample rate detect control register
Offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	MUTE_EN	If detect sample rate or channel width changing, mute the TX output as 0. 1: mute 0: not mute	R/W	0x0
11:9	-	Reserved	R/W	0x0
8	SRD_IE	Sample rate detect result change interrupt enable 0: disable 1: enable If sample rate detection module timeout, or detected sample rate changing or detected channel width changing, if would cause interrupt.	R/W	0x0
7:6	-	reserved	R/W	0x0
5:4	CNT_TIM	Slave mode sample rate detect counter period select 0: 2 LRCLK cycle 1: 4 LRCLK cycle Other: reserved	R/W	0x0
3:1	SRD_TH	These bits represent the sensitivity of sampling rate detection. SRC_PD interrupt will be triggered when the difference between CNT and previous detection results exceeds the preset value. 0: 8 1: 16 … 6: 56 7: 64 Value=(SRD_TH+1)*8	R/W	0x0
0	SRD_EN	Slave mode sample rate detect enable 0: disable 1: enable	R/W	0x0

11.3.7.6 I2STX_RDSTA

I2STX sample rate detect status register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0x0
24:12	CNT	CNT of LRCLK which sampling by SRC_CLK. CNT= Freq_ SRC_CLK / LRCLK. It would clear when module was enabling at first time.	R	0x0
11	TO_PD	Sample rate detect result timeout interrupt pending 0: no irq	R/W	0x0

		1: irq Write '1' to clean this bit. CNT overflow (0x9c00) would cause this irq.		
10	SRC_PD	Sample rate detect result sample rate change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
9	-	Reserved	R	0x0
8	CHW_PD	Sample rate detect result channel width change interrupt pending 0: no irq 1: irq Write '1' to clean this bit.	R/W	0x0
7:2	-	Reserved	R	0x0
1:0	WL	Channel word length (the rate of BCLK to LRCLK) 00: 16bit(32 rate) 01: 32bit(64 rate) 1x: Others	R	0x0

11.3.7.7 I2STX_FIFO_CNT

I2STX FIFO counter register
Offset = 0x20

Bit (s)	Name	Description	Access	Reset
31:19	-	Reserved	R	0x0
18	IP	I2STX FIFO sample counter overflow IRQ pending 0: no pending 1: pending Write '1' to clear this bit	R/W	0x0
17	IE	I2STX FIFO sample counter overflow IRQ enable 0: disable 1: enable If CNT overflow, it would cause an interrupt.	R/W	0x0
16	EN	I2STX FIFO counter enable 0:disable 1:enable Disable this function could reset the whole counter.	R/W	0x0
15:0	CNT	I2STX FIFO sample counter If overflow count would be clear to zero and cause an interrupt This counter count the valid data output by FIFO, it means that if FIFO is empty, this counter would not add till FIFO had been written data in again.	R	0x0

11.4 SPDIF TX

11.4.1 Features

SPDIF transmission (TX) supports sample rate 96k/48k/44.1k/32kHz.

11.4.2 SPDIF TX Register List

Table 11-7 SPDIFTX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPDIFTX_Control_Register	0xC0053000	0xC0053000

Table 11-8 SPDIFTX Controller Registers

Offset	Register Name	Description
0x00	SPDTX_CTL	SPDIFTX Control Register
0x04	SPDTX_CSL	SPDIFTX Channel State Low Register
0x08	SPDTX_CSH	SPDIFTX Channel State High Register

11.4.3 SPDIF TX Register Description

11.4.3.1 SPDTX_CTL

SPDIFTX Control Register
Offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	VALIDITY	Validity flag sent by hardware 0: Disable 0: Enable	R/W	0x0
1	SPD_DIS_CTL	0: Disable SPDIF (write 0 to SPDTX_CTL[0]) will take effect immediately. 1: Disable SPDIF (write 0 to SPDTX_CTL[0]) will take effect after the end of the right channel frame.	R/W	0x0
0	SPDEN	SPDIFTX Enable 0: Disable (will reset TX state machine) 1: Enable	R/W	0x0

11.4.3.2 SPDTX_CSL

SPDIFTX Channel State Low Register
Offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:0	SPDCSL	SPDIFTX Channel State Low (Channel state bit31 to bit0)	R/W	x

11.4.3.3 SPDTX_CSH

SPDIFTX Channel State High Register
Offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	SPDCSH	SPDIFTX Channel State High (Channel state bit47 to bit32)	R/W	x

11.5 SPDIF RX

11.5.1 Features

SPDIF receiver (RX) supports sample rate of 96k/48k/44.1k/32kHz.

11.5.2 SPDIF RX Register List

Table 11-9 SPDIFRX Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
SPDIFRX_Control_Register	0xC0054000	0xC0054000

Table 11-10 SPDIFRX Controller Registers

Offset	Register Name	Description
0x0000	SPDIFRX_CTL0	SPDIFRX Control0 Register
0x0004	SPDIFRX_CTL1	SPDIFRX Control1 Register
0x0008	SPDIFRX_CTL2	SPDIFRX Control2 Register
0x000C	SPDIFRX_PD	SPDIFRX IRQ Pending Register
0x0014	SPDIFRX_CNT	SPDIFRX CNT Register
0x0018	SPDIFRX_CSL	SPDIFRX Channel State Register
0x001C	SPDIFRX_CSH	SPDIFRX Channel State Register
0x0020	SPDIFRX_SAMP	SPDIFRX Sample Rate Detect Register
0x0024	SPDIFRX_SRTO_THRES	SPDIFRX Sample Rate Detect Timeout Threshold Register

11.5.3 SPDIF RX Register Description

11.5.3.1 SPDIFRX_CTL0

SPDIFRX Control0 Register
Offset=0x00

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R/W	0x0
14	VBM	Validity bit mask 0: disable 1: enable	R/W	0x0
13	DAMS	Data mask state 0: not mask 1: mask	R/W	0x0
12	DAMEN	If sample rate change the new data mask 0: disable 1: enable	R/W	0x0
11:8	DELTAADD	Delta_t_add Delta to Add on Configured or detected T Width	R/W	0x0
7:4	DELTAMIN	Delta_t_min	R/W	0x0

		Delta to minus from Configured or detected T Width		
3	DELTA_MODE	Setting ±delta for T Width 0: Soft mode, using the DELTAADD and DELTAMIN as ±delta. (The setting values of DELTAAD and DDELTAMIN should be greater than or equal to 3) 1: Hardware mode, The hardware compares 1.5T-1T differenceΔt1 with 2T-1.5T differenceΔt2, chooses half of the smallest Δt as ±delta, and updates it to DELTAADD and DELTAMIN registers. (But when $\frac{1}{2}$ Δt > 15, delta is 15) If BMC Decoder Err appears, the T value and delta will be updated after 256 change edges are received.	R/W	0x1
2	CAL_MODE	Cal_Mode 0: SoftWare Config T Width 1: HardWare Detect T Width	R/W	0x1
1	SPDIF_CKEDG	Select of SPDIF input signal latch clock edge 0: pos_edge 1: nege_edge	R/W	0x0
0	SPDIF_RXEN	SPDIF RX Enable 0: Disable 1: Enable	R/W	0x0

11.5.3.2 SPDIFRX_CTL1

SPDIFRX Control1 Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	x
24:16	WID2TCFG	2T Width Configure Maximum count 512	R/W	0x0
15:8	WID1P5TCFG	1.5T Width Configure Maximum count 256	R/W	0x0
7:0	WID1TCFG	1T Width = BCM Code Width of Data '1' 1T Width Configure Maximum count 256	R/W	0x0

11.5.3.3 SPDIFRX_CTL2

SPDIFRX Control2 Register
Offset =0x08

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	R	x
27:18	WID4TCFG	4T Width Configure Maximum count 1024	R/W	0x0
17:9	WID3TCFG	3T Width Configure Maximum count 512	R/W	0x0
8:0	WID2P5TCFG	2.5T Width Configure Maximum count 512	R/W	0x0

11.5.3.4 SPDIFRX_PD

SPDIFRX IRQ pending Register
Offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:17	-	Reserved	R	0x0
16	BL_HEADPD	Block head detect pending Writing '1' to clear	R/W	0x0
15	-	Reserved	R	0x0
14	SRTOPD	Sample rate detect timeout interrupt pending Writing '1' to clear	R/W	0x0
13	CSSRUPPD	Channel state sample rate change IRQ pending Writing '1' to clear	R/W	0x0
12	CSUPPD	Channel state update irq pending Writing '1' to clear	R/W	0x0
11	SRCPD	Sample rate change pending, Writing '1' to clear	R/W	0x0
10	BMCERPD	BMC Decoder Errror Pending， Writing '1' to clear	R/W	0x0
9	SUBRCVPD	Sub-Frame Receive Error Pending, Writing '1' to clear	R/W	0x0
8	BLKRCVPD	Block Receive Error Pending, Writing '1' to clear	R/W	0x0
7	-	Reserved	R	0x0
6	SRTOEN	Sample rate detect timeout IRQ enable 0: disable 1: enable	R/W	0x0
5	CSSRCIRQEN	Channel state sample rate change IRQ enable 0: disable 1: enable	R/W	0x0
4	CSUPIRQEN	Channel state update IRQ enable 0: disable 1: enable	R/W	0x0
3	SRCIRQEN	SPDIF RX Sample rate change IRQ enable 0: disable 1: enable	R/W	0x0
2	BMCIRQEN	BMC Decoder Error IRQ enable 1: Enable 0: Disable	R/W	0x0
1	SUBIRQEN	Sub-Frame Receive Error IRQ enable 1: Enable 0: Disable	R/W	0x0
0	BLKIRQEN	Block Receive Error IRQ enable 1: Enable 0: Disable	R/W	0x0

11.5.3.5 SPDIFRX_CNT

SPDIFRX CNT Register
Offset = 0x14

Bit (s)	Name	Description	Access	Reset
31:25	-	Reserved	R	0
24:16	HWDMAX	Hardware Detected maximum Width	R	0x0
15:8	HWDMIN	Hardware Detected minimum Width	R	0xff
7:0	FRAMECNT	Audio Frame Counter	R	0x0

		192 Frames in every audio block, range from 0 to 191.		

11.5.3.6 SPDIFRX_CSL

SPDIFRX Channel Status Register
Offset = 0x18

Bit (s)	Name	Description	Access	Reset
31:0	SPDCSL	SPDIFRX Channel State Low (Channel state bit31 to bit0)	R	x

11.5.3.7 SPDIFRX_CSH

SPDIFRX Channel Status Register
Offset = 0x1C

Bit (s)	Name	Description	Access	Reset
31:16	-	Reserved	R	0
15:0	SPDCSH	SPDIFRX Channel State High (Channel state bit47 to bit32)	R	x

11.5.3.8 SPDIFRX_SAMP

SPDIFRX Sample Rate Detect Register
Offset = 0x20

Bit (s)	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	SAMP_VALID	Sample rate valid flag 0: no valid 1: valid	R	0x0
27:16	SAMP_CNT	SPDIFRX Sample rate counter detect by 24M clock	R	0x0
15:5	-	Reserved	R	0x0
4:1	SAMP_DELTA	Delta is used by SAMP_CNT to detect sample rate change or not	R/W	0x7
0	SAMP_EN	Sample rate detect enable 1: Enable 0: Disable	R/W	0x0

11.5.3.9 SPDIFRX_ SRTO_THRES

SPDIFRX Sample Rate Detect Timeout Threshold Register
Offset = 0x24

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:0	SRTO_THRES	The threshold to generate sample rate detect timeout signal.	R/W	0xfa00

12 User Interface (UI)

12.1 LCD Controller (LCDC)

12.1.1 Features

- RGB565 source data format
- Source data Transfer to FIFO by DMA
- Support 8-bit active (TFT) LCD panels with digital CPU input interface
- Support read and write operation

12.1.2 Function Description

- RGB888 to RGB565 conversion can convert 24bits RBG to 16bits RGB before translating to LCD Panel
- Source data is transferred to frame FIFO through DMA
- LCDC can transfer YCbCr444 or RGB565 format data by setting bit SDT of register LCD_CTL

12.1.3 External Memory Interface

The External Memory Interface supports 8-bit or 16-bit CPU LCD. It is used to sent command to CPU LCD and read data back from CUP LCD to LCDC.
CPU can write or read through EXTMEM_DATA to access the extended bus according to IFSEL of EXTMEM_CTL.
When it is set to 8bit interface, CPU writes or reads the lowest 8 bits of EXTMEM_DATA, the bus accesses the lower 8bit data bus. When it is set to 16bit interface, CPU writes or reads the lowest 16 bits of EXTMEM_DATA, the bus accesses the 16 bit data bus.

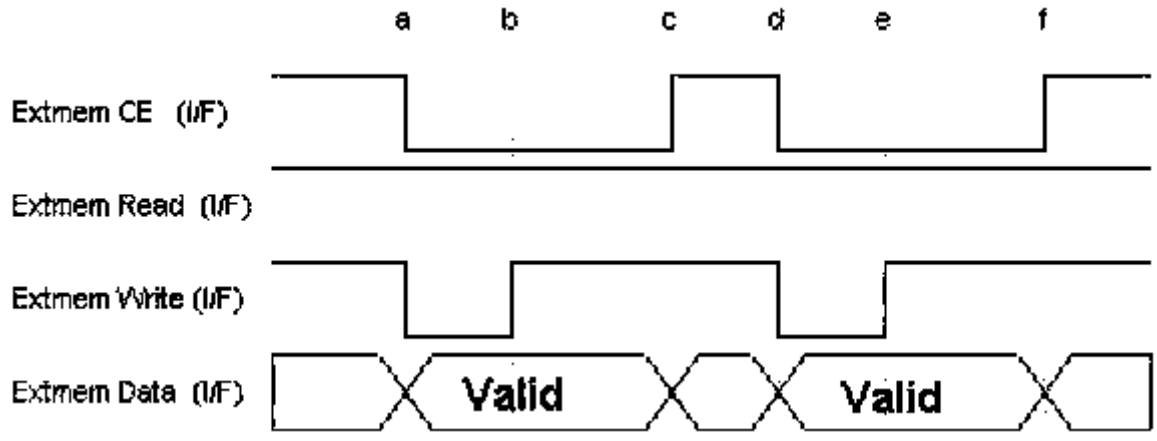


Figure 12-1 LCD Controller Write Timing

Write Timing:
a to b is the low state of writing cycle, the cycles depends on CLKLDU
b to c is the high state of writing cycle, the cycles depends on CLKHDU
a to c is a writing cycle,
When CPU writes EXTMEM_DATA register, the EXTMEM CEB is driven to low level, the host will drive the EXTMEM Data bus until the EXTMEM Write cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected.

The EXTMEM Write signal will be driven to low level until the low state counter is CLKLDU, then the write signal will be driven to high level until the high state counter is CLKHDU. The device will latch the data at the rise edge of EXTMEM Write.

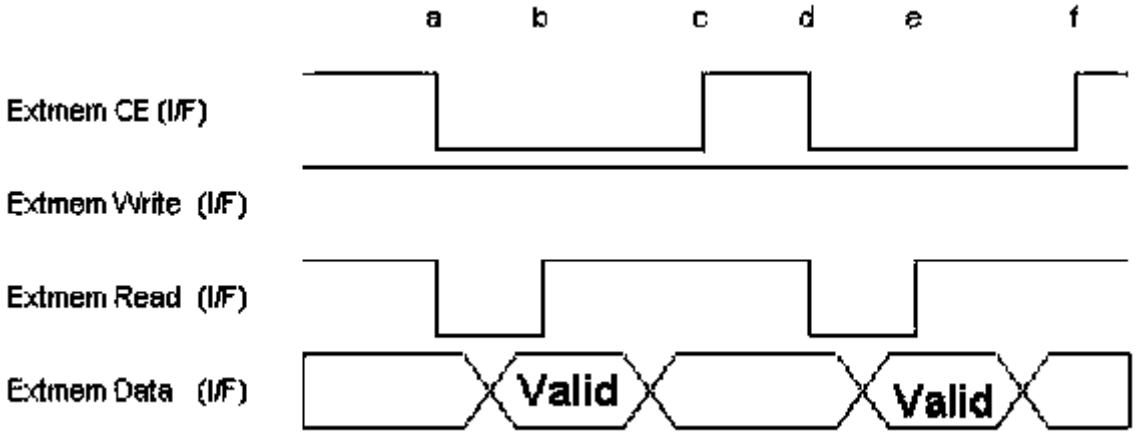


Figure 12-2 LCD Controller Read Timing

Read Timing:

a to b is the low state of reading cycle, the cycles depends on CLKLDU

b to c is the high state of reading cycle, the cycles depends on CLKHDU

a to c is a read cycle

When CPU reads EXTMEM_DATA register, the EXTMEM CEB is driven to low level until the EXTMEM Read cycle is over. When the EXTMEM CEB is low level, the LCM will be chip selected. The EXTMEM Read signal will be driven to low level until the low state counter is CLKLDU, then the read signal will be driven to high level until the high state counter is CLKHDU. When EXTMEM Read is low level, the LCM will drive the EXTMEM Data bus.

12.1.3.1 CPU IF timing

Table 12-1 Control signal define

RS	R/W	Function
0	0	Sets Index Register
0	1	Read Status
1	0	Writes Instruction
1	1	Reads Instruction

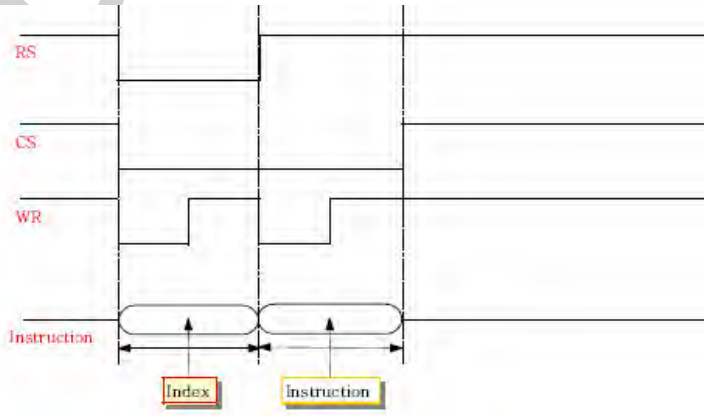


Figure 12-3 CPU LCD Timing

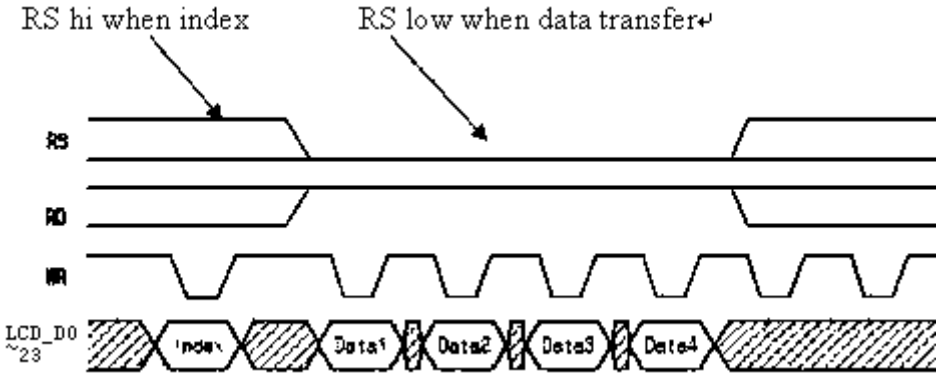


Figure 12-4 LCD Controller 8080 mode bus

12.1.4 LCD Register List

Table 12-2 LCD Controller Registers base address

Name	Physical Base Address	KSEG1 Base Address
LCDC_REGISTER	0xC0030000	0xC0030000

Table 12-3 RTC Controller Registers

Offset	Register Name	Description
0x0000	LCD_CTL	LCD Control Register
0x0004	LCD_CLKCTL	LCD and EXTMEM Clock adjust Register
0x0008	EXTMEM_CTL	Extended Memory Interface Control Register
0x000C	EXTMEM_CLKCTL	Extended Memory Interface Clock adjust Register
0x0010	EXTMEM_DATA	Extended Memory Interface DATA Register
0x0014	LCD_IF_PCS	LCD parity register

12.1.5 LCD Register Description

12.1.5.1 LCD_CTL

LCD controller control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	LCDFI	LCD Data translate Finish 0: busy 1: finish Writing '1' to clear the bit.	R/W	0x0
30:18	-	Reserved	R	0x0
17	FOVF	FIFO Overflow Pending Bit 0: Not overflow 1: overflow Writing '1' to clear this bit and reset the FIFO.	R/W	0x0
16:11	-	Reserved	R	0x0

10	FIFOET	FIFO Empty Status 0: Not Empty 1: Empty	R	0x0
9:8	-	Reserved	R	0x0
7	EMDE	FIFO Empty DRQ Enable 0: Disable 1: Enable This bit should be enabled when DMA is used to transmit the LCD data.	R/W	0x0
6:5	-	Reserved	R	0x0
4	FORMATS	RGB Format Select 0: 8bit (RGB 565 2transfer) 1:16bit (RGB 565 1transfer)	R/W	0x0
3	SEQ	RGB Sequence 0: RGB 1: BGR	R/W	0x0
2	MLS	When LCD_CTL[4](FORMATS) is '0', this bit is used to control LSB or MSB. 0: LSB 1: MSB	R/W	0x0
1	C86	Mode select 0: I8080 Interface 1: M6800 Interface	R/W	0x0
0	EN	LCD controller Enable 0: Disable 1: Enable Note: before setting this bit all other setting of LCDC should be set. This bit would be cleared by hardware after AHB Clock is synchronized with LCD Clock.	R/W	0x0

12.1.5.2 LCD_CLKCTL

LCD and EXTMEM Clock adjust Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:22	-	Reserved	R	0x0
21:16	CLKHDU	Clock High Level Duration (from LCD_CLK) from 1 to 64 (CLKHDU +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	CLKL2DU	Clock Low Level Duration (from LCD_CLK) from 1 to 64 (CLKL2DU +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	CLKLDU	Clock Low Level Duration (from LCD_CLK) from 1 to 64 (CLKLDU +1)	R/W	0xf

12.1.5.3 EXTMEM_CTL

Extended Memory Interface Control Register
Offset=0x0008

Bits	Name	Description	Access	Reset

31:29	CESEL	Choose the Chip Select of extended memory Interface 001: CE0 010: CE1 011: CE2 100: CE3 101: CE4 Others: Reserved Note: Write or read from LCDM， must select CE4.	R/W	0x5
28:9	-	Reserved	R	0x0
8	IFSEL	Choose the 8bits/16bits bus interface 0: 8 bits interface 1: 16 bits interface	R/W	0x0
7:1	-	Reserved	R	0x0
0	RS	RS select 0: RS output low voltage level 1: RS output high voltage level RS is low or high voltage in the case of writing INDEX/DATA/REG in different LCM.	R/W	0x0

12.1.5.4 EXTMEM_CLKCTL

EM clock control register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:22	-	Reserved	R	0x0
21:16	EXCLKH	Clock High Level Duration (from AHB_CLK) from 1 to 64 (EXCLKH +1)	R/W	0xf
15:14	-	Reserved	R	0x0
13:8	EXCL2KL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCL2KL +1)	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	EXCLKL	Clock Low Level Duration (from AHB_CLK) from 1 to 64 (EXCLKL +1)	R/W	0xf

NOTE: EXTMEM use clock from AHB_CLK, when use EXTMEM to sent command to LCDM or read data from LCDM, this register should be set to obtain perfect operation clock.

12.1.5.5 EXTMEM_DATA

Extended Memory Interface DATA Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:8	EXT_DATAH	The higher 8bit data bus of extended interface	R/W	0x0
7:0	EXT_DATAL	The lower 8bit data bus of extended interface	R/W	0x0

12.1.5.6 LCD_IF_PCS

LCD parity register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0

7:0	PCS	Parity Check Sum The Parity Check Sum of the LCD parallel interface (both 8 bit and 16bit).	R	0x0

12.2 SEG_LCD&LED controller

12.2.1 Features

- Support 3com / 4com / 5com / 6com SEG_LCD Driving Timing
- Support 4com or 8com DIG_LED Driving Timing
- Support 7 / 8 pin matrix_LED driving timing
- Support LED segment analog constant current configuration
- Support HOSC / LOSC for SEG_LCD & DIG_LED clock source

12.2.2 SEG_SREEN Register List

Table 12-4 SEG_SREEN Registers base address

Name	Physical Base Address	KSEG1 Base Address
SEG_SREEN	0xC00E0000	0xC00E0000

Table 12-5 SEG_SREEN Registers

Offset	Register Name	Description
0x0000	SEG_SREEN_CTL	Seg LCD Control Register
0x0004	SEG_SREEN_DATA0	Seg LCD Data Register0
0x0008	SEG_SREEN_DATA1	Seg LCD Data Register1
0x000C	SEG_SREEN_DATA2	Seg LCD Data Register2
0x0010	SEG_SREEN_DATA3	Seg LCD Data Register3
0x0014	SEG_SREEN_DATA4	Seg LCD Data Register4
0x0018	SEG_SREEN_DATA5	Seg LCD Data Register5
0x001C	SEG_RC_EN	LED SEG Restrict Current Enable Register
0x0020	SEG_BIAS_EN	LED SEG Bias Current Enable Register

12.2.3 SEG_SREEN Register Description

12.2.3.1 SEG_SREEN_CTL

Seg-screen control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	LCD_POWER	LCD POWER BACK DOOR 0: SEG0/SEG1 are used as normal function 1: When SEG0/SEG1 are selected as LCD_SEG function，SEG0/SEG1 output 1⁄3VCC and 2⁄3VCC Separately.	R/W	0x0
30:11	-	Reserved	R	0x0

10:8	LED_COM_DZ	The com of LED will got a “dead zone”, this register define the width of the dead zone: 000b: no dead zone between LED COM Beats 001b: 1/32 of the LED COM beat will be dead zone 010b: 2/32 of the LED COM beat will be dead zone 011b: 3/32 of the LED COM beat will be dead zone 100b: 4/32 of the LED COM beat will be dead zone 101b: 5/32 of the LED COM beat will be dead zone 110b: 6/32 of the LED COM beat will be dead zone 111b: 7/32 of the LED COM beat will be dead zone	R/W	0x0
7	SEGOFF	Segment Off 0: Segment is always off 1: Segment value is according to LCD_DATA P.S. Only active in COM/SEG or Digit-LED Mode	R/W	0x0
6	-	Reserved	R	0x0
5	LCD_OUT_EN	LCD&LED pad output Enable select 0: the pads of seg_LCD and LED will output “high_Z”. 1: the pads of seg_LCD and LED output signal as it’s timing.	R/W	0x0
4	REFRSH	Refresh LCD/LED Data 0: Hold LCD_DATA Refresh LCD/LED panel according to the LCD_DATA buffer value 1: Update LCD_DATA Refresh the LCD_DATA buffer value from LCD_DATA register P.S. Only active in COM/SEG or Digit-LED Mode; When updating the value of LCD_DATA register, write “1” to this bit, the hardware will clear this bit when the LCD_DATA has been updated.	R/W	0x0
3:0	MODE_SEL	Mode Select 0000b: 3Com,1/3 Bias SEG/COM LCD Frame-Invert 0001b: 3Com,1/3 Bias SEG/COM LCD Row-Invert 0010b: 4Com,1/3 Bias SEG/COM LCD Frame-Invert 0011b: 4Com,1/3 Bias SEG/COM LCD Row-Invert 0100b: 5Com,1/3 Bias SEG/COM LCD Frame-Invert 0101b: 5Com,1/3 Bias SEG/COM LCD Row-Invert 0110b: 6Com,1/3 Bias SEG/COM LCD Frame-Invert 0111b: 6Com,1/3 Bias SEG/COM LCD Row-Invert 1000b: 4Com Digit-LED Common-Cathode Mode 1001b: 4Com Digit-LED Common- Anode Mode 1010b: 8Com Digit-LED Common-Cathode Mode 1011b: 8Com Digit-LED Common- Anode Mode 1100b: 7Pin Matrix_LED Common-Cathode mode 1101b: 7Pin Matrix_LED Common- Anode mode 1110b: 8Pin Matrix_LED Common-Cathode mode 1111b: 8Pin Matrix_LED Common- Anode mode	R/W	0x0

12.2.3.2 SEG_SREEN_DATA0

Seg-screen data register0
Offset=0x0004

Bits	Name	Description	Access	Reset

31:24	COM0_BYTE3	SEG/COM Mode:COM0_SEG[31:24] Digit-LED Mode:COM3_seg[7:0] Matrix_LED: COM3_seg[7:0] When set to “1”, the cross of COM and SEG is ON; Else is OFF.	R/W	0x0
23:16	COM0_BYTE2	SEG/COM Mode:COM0_SEG[23:16] Digit-LED Mode:COM2_seg[7:0] Matrix_LED: COM2_seg[7:0]	R/W	0x0
15:8	COM0_BYTE1	SEG/COM Mode:COM0_SEG[15:8] Digit-LED Mode:COM1_seg[7:0] Matrix_LED: COM1_seg[7:0]	R/W	0x0
7:0	COM0_BYTE0	SEG/COM Mode:COM 0_SEG[7:0] Digit-LED Mode:COM0_seg[7:0] Matrix_LED: COM0_seg[7:0]	R/W	0x0

12.2.3.3 SEG_SREEN_DATA1

Seg-screen data register1
Offset=0x0008

Bits	Name	Description	Access	Reset
31:24	COM1_BYTE3	SEG/COM Mode:COM1_SEG[31:24] Digit-LED Mode:COM7_seg[7:0] Matrix_LED: COM7_seg[7:0]	R/W	0x0
23:16	COM1_BYTE2	SEG/COM Mode:COM1_SEG[23:16] Digit-LED Mode:COM6_seg[7:0] Matrix_LED: COM6_seg[7:0]	R/W	0x0
15:8	COM1_BYTE1	SEG/COM Mode:COM1_SEG[15:8] Digit-LED Mode:COM5_seg[7:0] Matrix_LED:COM5_seg[7:0]	R/W	0x0
7:0	COM1_BYTE0	SEG/COM Mode:COM1_SEG[7:0] Digit-LED Mode:COM4_seg[7:0] Matrix_LED: COM4_seg[7:0]	R/W	0x0

12.2.3.4 SEG_SREEN_DATA2

Seg-screen data register2
Offset=0x000C

Bits	Name	Description	Access	Reset
31:0	COM2_WORD	SEG/COM Mode:COM2_SEG[31:0] if the xTH bit of this register is “1”, Com2_seg-x will on.	R/W	0x0

12.2.3.5 SEG_SREEN_DATA3

Seg-screen data register3
Offset=0x0010

Bits	Name	Description	Access	Reset
31:0	COM3_WORD	SEG/COM Mode:COM3_SEG[31:0] if the xTH bit of this register is “1”, Com3_seg-x will on.	R/W	0x0

12.2.3.6 SEG_SREEN_DATA4

Seg_screen data register4
Offset=0x0014

Bits	Name	Description	Access	Reset
31:0	COM4_WORD	SEG/COM Mode:COM4_SEG[31:0] if the xTH bit of this register is “1”, Com4_seg-x will on.	R/W	0x0

12.2.3.7 SEG_SREEN_DATA5

Seg_screen data register5
Offset=0x0018

Bits	Name	Description	Access	Reset
31:0	COM5_WORD	SEG/COM Mode:COM5_SEG[31:0] if the xTH bit of this register is “1”, Com5_seg-x will on.	R/W	0x0

12.2.3.8 SEG_RC_EN

LED SEG Restrict Current Enable
Offset=0x1C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	LED_SEG7	LED SEG7 Restrict Current Enable	R/W	0x0
6	LED_SEG6	LED SEG6 Restrict Current Enable	R/W	0x0
5	LED_SEG5	LED SEG5 Restrict Current Enable	R/W	0x0
4	LED_SEG4	LED SEG4 Restrict Current Enable	R/W	0x0
3	LED_SEG3	LED SEG3 Restrict Current Enable	R/W	0x0
2	LED_SEG2	LED SEG2 Restrict Current Enable	R/W	0x0
1	LED_SEG1	LED SEG1 Restrict Current Enable	R/W	0x0
0	LED_SEG0	LED SEG0 Restrict Current Enable	R/W	0x0

12.2.3.9 SEG_BIAS_EN

LED SEG Bias Current Enable
Offset=0x20

Bits	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	LED_SEG_ALL_EN	LED SEG Restrict Current ALL Enable 0: Disable 1: Enable	R/W	0x0
3	LED_CATHODE_ANODE_MODE	LED Cathode/Anode Mode 0: Cathode Mode 1: Anode Mode	R	0x0
2:0	LED_SEG_BIAS	LED SEG BIAS 000: 2mA 001: 3mA 010: 6mA 011: 7mA 100: 10 mA 101: 11 mA 110: 14mA 111: 15mA	R/W	0x1

13 GPIO and I/O Multiplexer

13.1 Features

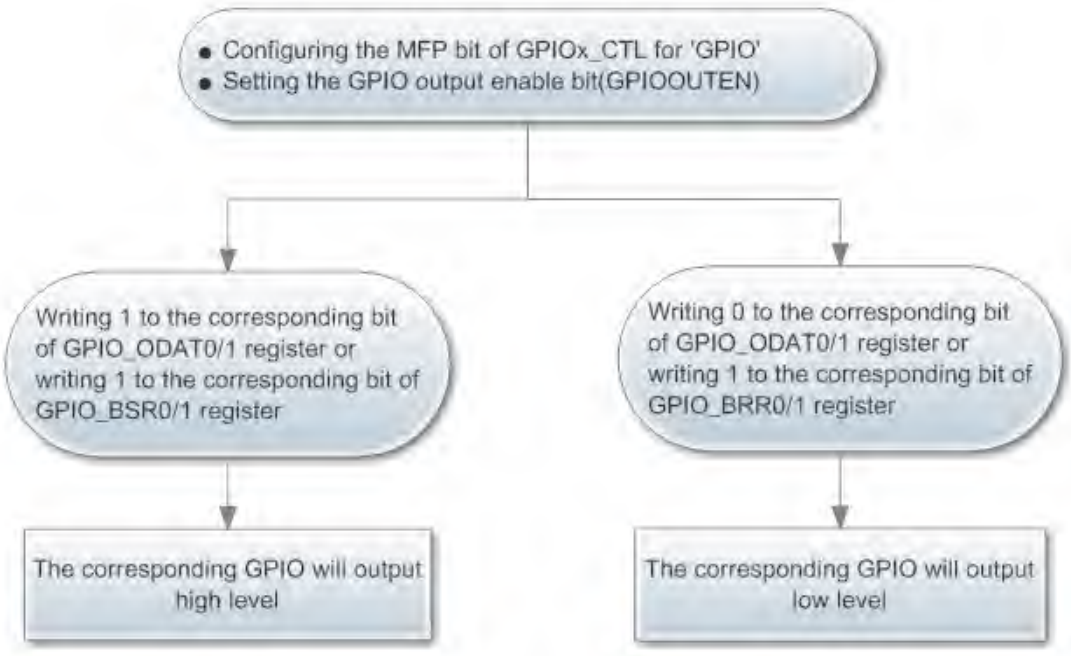
- Supports 31 Programmable GPIO , 1 WIO(wake up IO), and 12 analog IOs can also config as GPIOs.
- GPIO can output 0 or 1 and detect the signal level of the external circuit. Each GPIO has its own enable control bit and data registers.
- All GPIO and WIO has internal pull down or pull up resistors
- Driving strength can be adjusted, Level (n) corresponds to (2n) mA
- Automatically switching PAD function

13.2 Operation Manual

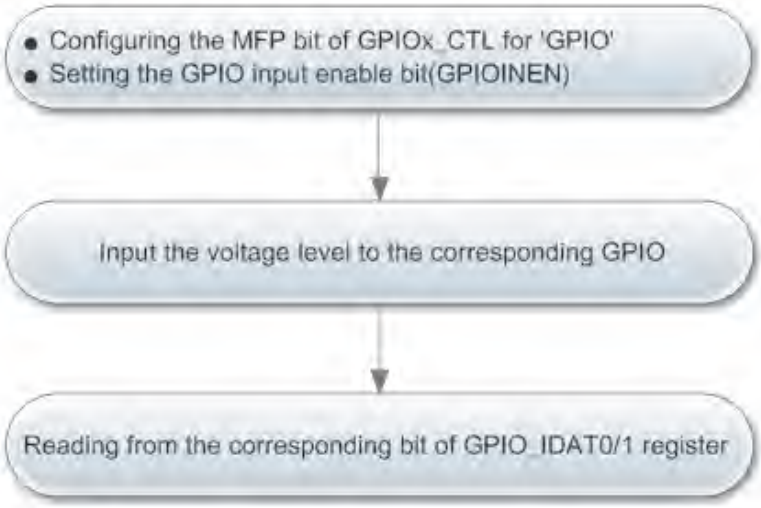
13.2.1 Multi-function Switch Operation

1. Some pin can be multiplexed as three kinds of functions: module function (MFP), GPIO function, Analog function, which can be configured by setting AD_Select bit and MFP bit of GPIOx_CTL registers.
2. GPIO and MFP are digital functions. Once the Analog function is selected, the digital functions will fail. The function priority of some multiplexed pin are Analog function > GPIO function > MFP function.
3. GPIO[44:55] can be multiplexed as analog function and digital function. If the pin is used as digital function, it must be disabled analog function firstly by setting AD_Select register.
4. Some MFP modules have itself pull-up and pull-down resistors, referring the chapter Pad PU control register and Pad PD control register; when the pin is multiplexed as MFP module function, the modules pull-up/pull-down resistors will be enabled automatically and the pull-up/pull-down resistors of GPIOs must be DISABLED, or the voltage level and functions will be abnormal.

13.2.2 GPIO Output

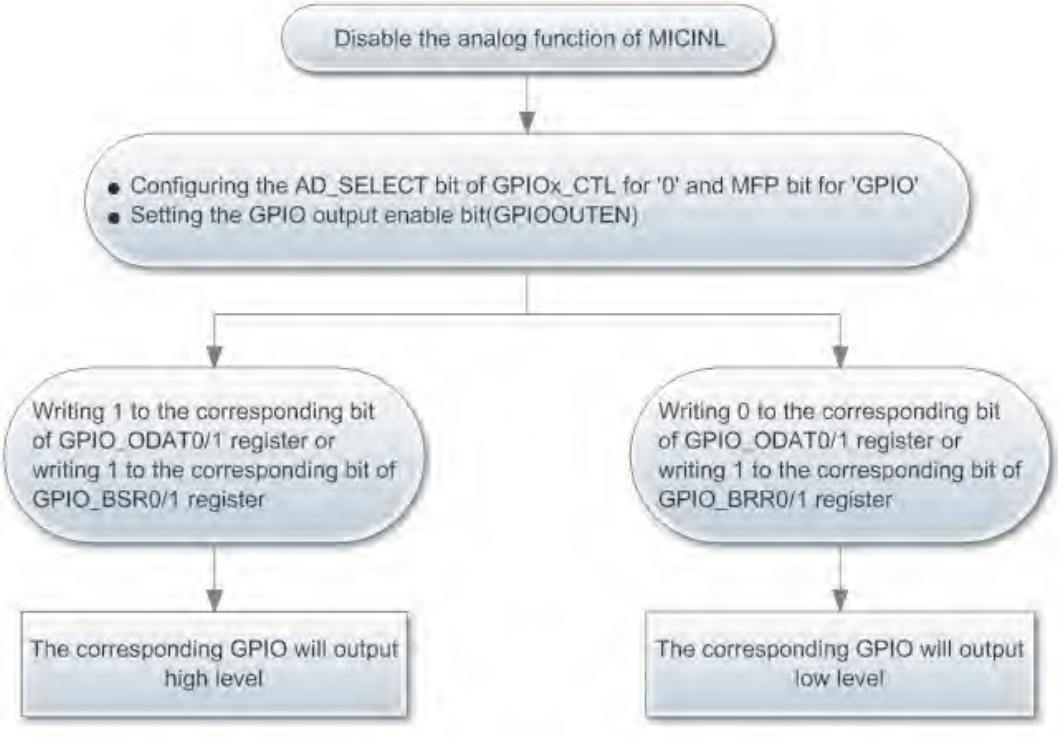


13.2.3 GPIO Input



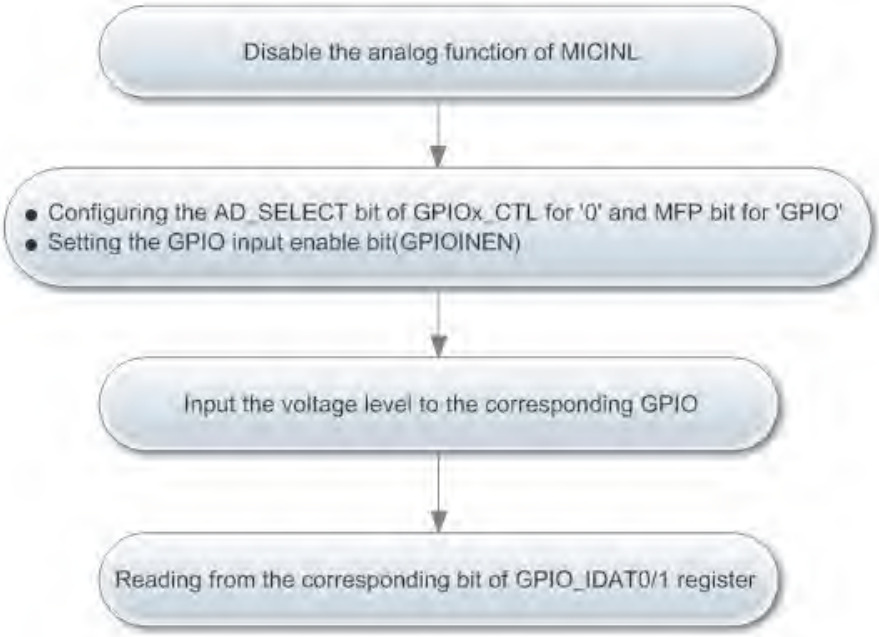
13.2.4 GPIO[44:55] Output

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as GPIO.

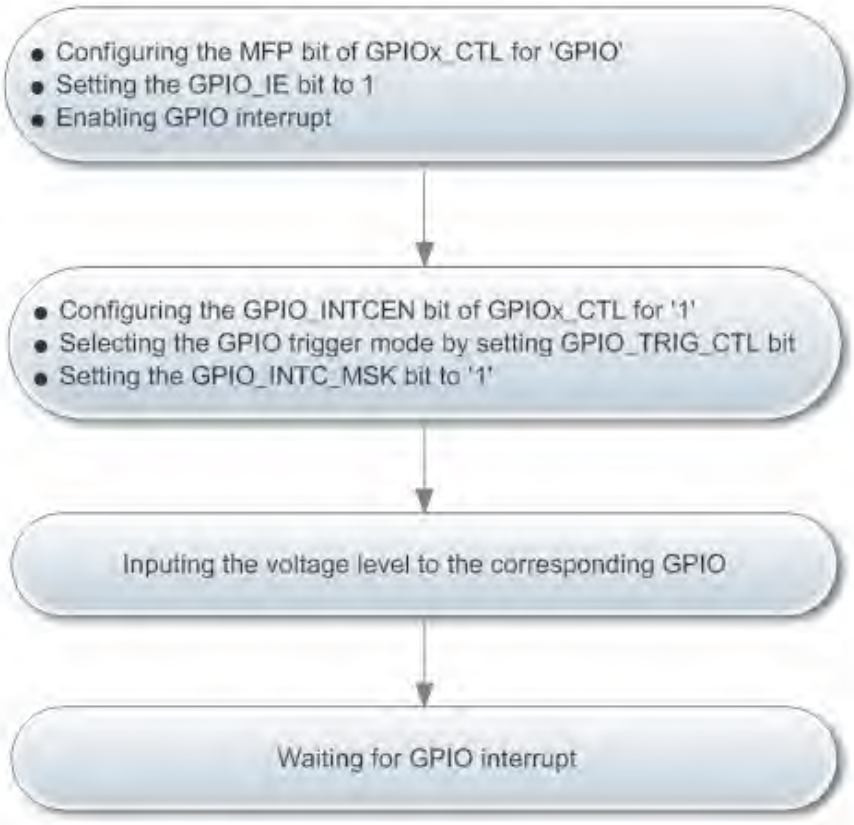


13.2.5 GPIO[44:55] Input

Refer to the procedure as follows to configure an analog pin MICINL as a digital function such as GPIO.



13.2.6 GPIO INTC



13.3 GPIO Register List

Table 13-1 GPIO_MFP Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
GPIO_MFP_REGISTER	0xC0090000	0xC0090000

Table 13-2 GPIO&MFP Controller Registers

Offset	Register Name	Description	Voltage
0x0004	GPIO0_CTL	GPIO0 control Register	VDD
0x0008	GPIO1_CTL	GPIO1 control Register	VDD
0x000C	GPIO2_CTL	GPIO2 control Register	VDD
0x0010	GPIO3_CTL	GPIO3 control Register	VDD
0x0014	GPIO4_CTL	GPIO4 control Register	VDD
0x0018	GPIO5_CTL	GPIO5 control Register	VDD
0x001C	GPIO6_CTL	GPIO6 control Register	VDD
0x0020	GPIO7_CTL	GPIO7 control Register	VDD
0x0024	GPIO8_CTL	GPIO8 control Register	VDD
0x0028	GPIO9_CTL	GPIO9 control Register	VDD
0x002C	GPIO10_CTL	GPIO10 control Register	VDD
0x0030	GPIO11_CTL	GPIO11 control Register	VDD
0x0034	GPIO12_CTL	GPIO12 control Register	VDD
0x0038	GPIO13_CTL	GPIO13 control Register	VDD
0x003C	GPIO14_CTL	GPIO14 control Register	VDD
0x0040	GPIO15_CTL	GPIO15 control Register	VDD
0x0044	GPIO16_CTL	GPIO16 control Register	VDD
0x0048	GPIO17_CTL	GPIO17 control Register	VDD
0x0050	GPIO19_CTL	GPIO19 control Register	VDD
0x0054	GPIO20_CTL	GPIO20 control Register	VDD
0x0058	GPIO21_CTL	GPIO21 control Register	VDD
0x005C	GPIO22_CTL	GPIO22 control Register	VDD
0x0060	GPIO23_CTL	GPIO23 control Register	VDD
0x0084	GPIO32_CTL	GPIO32 Control Register	VDD
0x0088	GPIO33_CTL	GPIO33 Control Register	VDD
0x008C	GPIO34_CTL	GPIO34 Control Register	VDD
0x0090	GPIO35_CTL	GPIO35 Control Register	VDD
0x009C	GPIO38_CTL	GPIO38 Control Register	VDD
0x00A0	GPIO39_CTL	GPIO39 Control Register	VDD
0x00A4	GPIO40_CTL	GPIO40 Control Register	VDD
0x00AC	GPIO42_CTL	GPIO42 Control Register	VDD
0x00B4	GPIO44_CTL	GPIO44 Control Register	VDD
0x00B8	GPIO45_CTL	GPIO45 Control Register	VDD
0x00BC	GPIO46_CTL	GPIO46 Control Register	VDD
0x00C0	GPIO47_CTL	GPIO47 Control Register	VDD
0x00C4	GPIO48_CTL	GPIO48 Control Register	VDD
0x00C8	GPIO49_CTL	GPIO49 Control Register	VDD
0x00CC	GPIO50_CTL	GPIO50 Control Register	VDD
0x00D0	GPIO51_CTL	GPIO51 Control Register	VDD
0x00D4	GPIO52_CTL	GPIO52 Control Register	VDD
0x00D8	GPIO53_CTL	GPIO53 Control Register	VDD
0x00DC	GPIO54_CTL	GPIO54 Control Register	VDD
0x00E0	GPIO55_CTL	GPIO55 Control Register	VDD
0x0100	GPIO_ODAT0	GPIO Output Data Register 0	VDD
0x0104	GPIO_ODAT1	GPIO Output Data Register 1	VDD
0x0108	GPIO_BSR0	GPIO Output Data bit Set Register 0	VDD
0x010C	GPIO_BSR1	GPIO Output Data bit Set Register 1	VDD
0x0110	GPIO_BRR0	GPIO Output Data bit Reset Register 0	VDD
0x0114	GPIO_BRR1	GPIO Output Data bit Reset Register 1	VDD

0x0118	GPIO_IDAT0	GPIO Input Data Register 0	VDD
0x011C	GPIO_IDAT1	GPIO Input Data Register 1	VDD
0x0120	GPIO_PD0	GPIO IRQ Pending Register 0	VDD
0x0124	GPIO_PD1	GPIO IRQ Pending Register 1	VDD
0x0140	WIO0_CTL	WIO0 Control Register	RTCVDD

13.4 GPIO Register Description

13.4.1 GPIO0_CTL

GPIO0 control Register
Offset=0x04

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010: dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable	R/W	0x0

		1: Enable		
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: Disable 1: Enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM0 0010: EM_WRB 0011: LCD_WRB 0100: LCD_COM0 0101: TWI_SCL 0110: PWM1 0111: UART0_RTS 1001: I2STX_MCLK 1010: I2SRX0_MCLK 1011: I2SRX1_MCLK 1100: TIMER2_CAP 1101: SPI2_SS Others: Reserved	R/W	0x0

13.4.2 GPIO1_CTL

GPIO1 control Register
Offset=0x08

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0

14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM1 0010: EM_RS 0011: LCD_RS 0100: LCD_COM1 0101: TWI_SDA 0110: PWM3 0111: UART0_CTS 1001: I2STX_BCLK 1010: I2SRX0_BCLK 1011: I2SRX1_BCLK 1100: TIMER3_CAP 1101:SPI2_MISO Others: Reserved	R/W	0x0

13.4.3 GPIO2_CTL

GPIO2 control Register
Offset=0x0C

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt	R/W	0x0

		to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect		
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM2 0010: EM_RDB 0011: LCD_RDB 0100: LCD_COM2 0101: SPI1_MOSI	R/W	0x0

		0110: PWM2 0111: UART0_RX 1000: LRADC4 1001: I2STX_LRCLK 1010: I2SRX0_LRCLK 1011: I2SRX1_LRCLK 1100: TIMER2_CAP 1101: SPI2_MOSI Others: Reserved		

13.4.4 GPIO3_CTL

GPIO3 control Register
Offset=0x10

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable	R/W	0x0

		0: Disable 1: Enable		
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM3 0010: EM_CEB0 0011: LCD_CEB 0100: LCD_COM3 0101: SPI1_SCLK 0111: UART0_TX 1001: I2STX_DOUT 1010: I2SRX0_DIN 1011: I2SRX1_DIN 1100: TIMER3_CAP 1101:SPI2_SCLK Others: Reserved	R/W	0x0

13.4.5 GPIO4_CTL

GPIO4 control Register
Offset=0x14

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0
23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is ‘1’.	R/W	0x0
19:15	-	Reserved	R	0x0

14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM4 0010: EM_CEB1 0011: LCD_CEB 0100: LCD_COM4 0110: PWM1 1100: TIMER2_CAP 1101: IR_RX 1111: VMIC Others: Reserved	R/W	0x0

13.4.6 GPIO5_CTL

GPIO5 control Register
Offset=0x18

Bit (s)	Name	Description	Access	Reset
31:26	-	Reserved	R	0x0
25	GPIO_INTC_MSK	GPIO INTC mask 0: Mask the interrupt, do not send the interrupt to the INTC module; 1: Send interrupt to the INTC，when the GPIO trigger event is detect	R/W	0x0
24	-	Reserved	R	0x0

23:21	GPIO_TRIG_CTL	GPIO trigger mode 000: rising edge 001: falling edge 010:dual edge 011: high level 100: low level Others: Reserved	R/W	0x0
20	GPIO_INTCEN	GPIO INTC Enable 0: Disable, do not generate IRQ pending and do not send IRQ to INTC. 1: Enable, generate IRQ pending when the GPIO trigger event is detect, and send IRQ to INTC when GPIO_INTC_MSK is '1'.	R/W	0x0
19:15	-	Reserved	R	0x0
14:12	PADDRV	GPIO PAD Drive Control 000: Level 1 001: Level 2 010: Level 3 011: Level 4 100: Level 5 101: Level 6 110: Level 7 111: Level 8	R/W	0x1
11	GPIO50KPUEN	GPIO 50K PU Enable 0: Disable 1: Enable	R/W	0x0
10	-	Reserved	R	0x0
9	GPIO100KPDEN	GPIO 100K PD Enable 0: Disable 1: Enable	R/W	0x0
8	GPIO10KPUEN	GPIO 10K PU Enable 0: Disable 1: Enable	R/W	0x0
7	GPIOINEN	GPIO Input Enable 0: Disable 1: Enable	R/W	0x0
6	GPIOOUTEN	GPIO Output Enable 0: Disable 1: Enable	R/W	0x0
5	SMIT	PAD Schmitt enable bit of GPIO 0: disable 1: enable	R/W	0x0
4	-	Reserved	R	0x0
3:0	MFP	Multi-Function of GPIO 0000: GPIO 0001: LED_COM5 0010: EM_CEB2 0011: BT_REQ 0100: LCD_COM5 0110: PWM3 1100: TIMER3_CAP Others: Reserved	R/W	0x0