7.4.17 LRADC7_DATA

LRADC7 DATA Register, offset = 0x7C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC7	LRADC7 data output LRADC7 input voltage range is 0 to 3.6V.	R	xx

7.4.18 LRADC8_DATA

LRADC8 DATA Register, offset = 0x80

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC8	LRADC8 data output LRADC8 input voltage range is 0 to 3.6V.	R	xx

7.4.19 LRADC9_DATA

LRADC9 DATA Register, offset = 0x84

Bit (s)	Name	Description	Access	Reset
31:10	-	RESERVED	R	0x0
9:0	LRADC9	LRADC9 data output LRADC9 input voltage range is 0 to 3.6V.	R	xx

7.4.20 LRADC10_DATA

LRADC10 DATA Register, offset = 0x88

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC10	LRADC10 data output LRADC10 input voltage range is 0 to 3.6V.	R	xx

7.4.21 LRADC11_DATA

LRADC11 DATA Register, offset = 0x8C

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	LRADC11	LRADC11 data output LRADC11 input voltage range is 0 to 3.6V.	R	xx

7.4.22 AVCCADC_DATA

AVCCADC DATA Register, offset = 0x90

Bit (s)	Name	Description	Access	Reset
31:10	-	Reserved	R	0x0
9:0	AVCCADC	AVCCADC data output AVCCADC input voltage range is 0 to 3.6V.	R	xx

8 System Control

8.1 RMU

8.1.1 Features

The RMU Controller of ATS2835P has following features:

- The RMU (Reset Management Unit) can reset all the peripherals.
- The MCU can enter power-saving mode by setting the registers of RMU.

8.1.2 RMU Register List

Table 8-1 RMU base address

Name	Physical Base Address	KSEG1 Base Address
RMU	0xC0000000	0xC0000000

Table 8-2 RMU register list

Offset	Register Name	Description
0x0000	MRCR0	Module Reset Control Register0
0x0004	MRCR1	Module Reset Control Register1
0x0008	DSP_VCT_ADDR	DSP_VECTOR_ADDRESS Register

8.1.3 RMU Register Description

8.1.3.1 MRCR0

Module Reset Control Register0, offset = 0x0000

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R/W	0x0
29	SPI2RESET	SPI2 Controller Reset 0: reset 1: normal	R/W	0x0
28:27	-	Reserved	R	0x0
26	IRRESET	IR Controller Reset 0: reset 1: normal	R/W	0x0
25	-	Reserved	R	0x0
24	USBRESET2	This bit should be reset before USBReset bit is reset. 0: reset 1: normal	R/W	0x0
23	USBRESET	USB Reset 0: reset 1: normal	R/W	0x0
22	-	Reserved	R	0x0
21	PWM_RESET	PWM Reset 0: reset 1: normal	R/W	0x0
20	-	Reserved	R	0x0

19	SEGLCDRESET	SEGLCD & SEGLED Controller Reset 0: reset 1: normal	R/W	0x0
18	LCDRESET	LCD controller Reset 0: reset 1: normal	R/W	0x0
17	TWIRESET	TWI Controller Reset 0: reset 1: normal	R/W	0x0
16	UART1RESET	UART1 Controller Reset 0: reset 1: normal	R/W	0x0
15	UART0RESET	UART0 Controller Reset 0: reset 1: normal	R/W	0x0
14	SPI1DCACHERESET	SPI1DCache Controller Reset 0: reset 1: normal	R/W	0x0
13	SPI0CACHERESET	SPICache Controller Reset 0: reset 1: normal	R/W	0x0
12	SPI1RESET	SPI1 Controller Reset 0: reset 1: normal	R/W	0x0
11	SPI0RESET	SPI0 Controller Reset 0: reset 1: normal	R/W	0x0
10	SD1RESET	SD1 Card Controller Reset 0: reset 1: normal	R/W	0x0
9	SD0RESET	SD0/MMC Card Controller Reset 0: reset 1: normal	R/W	0x0
8	AUDIOIORESET	Audio Global Reset 0: reset 1: normal	R/W	0x0
7	-	Reserved	R	0x0
6	SPDIFTXREAST	SPDIFTX Reset 0: reset 1: normal	R/W	0x1
5	SPDIFRXREAST	SPDIFRX Reset 0: reset 1: normal	R/W	0x1
4	I2SRESET	I2S Reset 0: reset 1: normal	R/W	0x1
3	ADCRESET	ADC Reset 0: reset 1: normal	R/W	0x1
2	DACRESET	DAC Reset 0: reset 1: normal	R/W	0x1
1	-	Reserved	R	0x0

0	DMARESET	DMA0 ~ DMA7 Reset 0: reset 1: normal The reset bit of DMA controller is active while it is driven by MCU clock.	R/W	0x0

8.1.3.2 MRCR1

Module Reset Control Register1, offset = 0x0004

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R/W	0x0
29	DSP_PART	All but OCEM DSP reset 0: reset DSP except OCEM（debug only） 1: normal Debug using only, do not set to 0.	R/W	0x1
28	DSP_ALL	All DSP reset 0: reset all dsp 1: depends on DSP_PART	R/W	0x0
27:0	-	Reserved	R/W	0x0

8.1.3.3 DSP_VCT_ADDR

DSP Vector Address Register, offset = 0x0008

Bit (s)	Name	Description	Access	Reset
31:0	DSP_VECTOR_ADDRESS	DSP_VECTOR_ADDRESS	R/W	0x4000

8.2 CMU Analog

8.2.1 Features

- Support only one oscillator inputs: 24MHz
- Supply 4 PLLs and special clocks of all modules. The 4 PLLs are CORE PLL, SPLL, Audio PLL0 and Audio PLL1

8.2.2 CMU Analog Register List

Table 8-3 CMU Analog Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_ANALOG_REGISTER	0xC0000100	0xC0000100

Table 8-4 CMU Analog Controller Registers

Offset	Register Name	Description
0x00	HOSC_CTL	HOSC control register
0x04	CORE_PLL_CTL	CORE_PLL Control Register
0x08	SPLL_CTL	SPLL Control Register
0x0C	AUDIO_PLL0_CTL	AUDIO PLL0 Control Register
0x10	AUDIO_PLL1_CTL	AUDIO PLL1 Control Register

8.2.3 CMU Analog Register Description

8.2.3.1 HOSC_CTL

HOSC control register, offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:27	-	Reserved, be read as zero.	R	0x0
26:24	HOSCI_BC_SEL	HOSCI PAD base cap select 000: 0p 001: 3p 010: 6p 011: 9p 100: 12p 101: 15p** 110: 18p 111: 21p	R/W	0x5
23:19	HOSCI_TC_SEL	HOSCI PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCI_TC_SEL	R/W	0x0
18:16	HOSCO_BC_SEL	HOSCO PAD base cap select 000: 0p 001: 3p 010: 6p 011: 9p 100: 12p 101: 15p** 110: 18p 111: 21p	R/W	0x5
15:11	HOSCO_TC_SEL	HOSCO PAD trim cap select, range from 0pF to 3.1pF Trim cap = 0.1pF * HOSCO_TC_SEL	R/W	0x0
10:6	HGMC	High Frequency crystal Oscillator GMMIN select bits	R/W	0x1f
5	BT_HOSC_SEL	BT HOSC clock select 0: BT_HOSC clock select smiths trigger output. 1: BT_HOSC clock select buffer output. This bit is valid for HOSC from the source, not only valid for HOSC to BT.	R/W	0x0
4	VDD_HOSC_SEL	VDD_HOSC clock select 0: select HOSC before GHR 1: select HOSC after GHR Glitch in HOSC low than 3ns will be removed by GHR. The glitch remove clock only provide to VDD power domain;	R/W	0x1
3:1	-	Reserved	R	0x0
0	HOSC_EN	HOSC enable 0: disable 1: enable Only this bit in the register in the VDD domain. When S3 is active by hardware, HOSC will be disabled automatically, insurance lower power consumption in S3 state.	R/W	0x1

8.2.3.2 CORE_PLL_CTL

CORE_PLL Control Register, offset = 0x04

Bit (s)	Name	Description	Access	Reset
31:14	-	Reserved, be read as zero.	R	0x0
13	COREPLL_SAFETUNE_EN	COREPLL output frequency safe tune en	R/W	0x1
12	COREPLL_HSAFE	COREPLL output frequency high safe tune Bit 0: low safe 1:high safe	R/W	0x1
11:9	-	Reserved, be read as zero.	R	0x0
8	CORE_PLL_PMD	CORE PLL phase match detect 0: CORE PLL phase not match 1: CORE PLL phase match	R	X
7	CORE_PLL_EN	CORE PLL Enable 0: Disable 1: Enable	R/W	0x0
6:0	SCORE	CORE PLL Frequency Select: Formula: 6M* SCORE Range:36 ~ 378M Value must be bigger than 6 0-5: reserved 6: 6*6M=36M …… 63: 63*6M=378M Others: reserved.	R/W	0x06

8.2.3.3 SPLL_CTL

SPLL Control Register, offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	CK32M_EN	SPLL 32M clock gating 0: disable 1: enable	R/W	0x1
3:2	CK32M_DUTY	SPLL 32M CLOCK duty select 00: 25.0% 01: 37.5% 1x:50%	R/W	0x1
1	SPLL_LOCK	SPLL phase match detect 0: SPLL phase not match 1: SPLL phase match	R	X
0	SPLL_EN	SPLL Enable 0: disable 1: enable	R/W	0x0

8.2.3.4 AUDIO_PLL0_CTL

AUDIO PLL Control Register, offset = 0x0C

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5	AUDIO_PLL0_MODE	AUDIO PLL0 Mode selection	R/W	0x1

		0: Mode0 1: Mode1		
4	AUDPLL0EN	Audio PLL0 Enable 0: Disable 1: Enable	R/W	0x0
3:0	APS0	AUDIO PLL0 Clock Selection	R/W	0x0

8.2.3.5 AUDIO_PLL1_CTL

AUDIO PLL1 Control Register, offset = 0x10

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5	AUDIO_PLL1_MODE	AUDIO PLL1 Mode selection 0: Mode0 1: Mode1	R/W	0x1
4	AUDPLL1EN	Audio PLL1 Enable 0: Disable 1: Enable	R/W	0x0
3:0	APS1	AUDIO PLL1 Clock Selection	R/W	0x0

8.3 CMU Digital

8.3.1 Features

The CMU (Clock Management Unit) can select HOSC, CORE_PLL, CK3M and CK32K as the clock of each peripheral.

8.3.2 CMU Digital Register List

Table 8-5 CMU Digital Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
CMU_DIGITAL_REGISTER	0xC0001000	0xC0001000

Table 8-6 CMU Digital Controller Registers

Offset	Register Name	Description
0x0000	CMU_SYSCLK	SYSCLK Control Register
0x0004	CMU_DEVCLKEN0	DEVCLKEN Control Register0
0x0008	CMU_DEVCLKEN1	DEVCLKEN Control Register1
0x0014	CMU_ADDACLK	ADDACLK Control Register
0x0018	CMU_I2SCLK	I2SCLK Control Register
0x001C	CMU_SPDIFCLK	SPIDIFCLK Control Register
0x0020	CMU_SDCLK	SD0/1 CLK Control Register
0x0024	CMU_SPICLK	SPI0/1 CLK Control Register
0x0028	CMU_IRCLK	IR CLK Control Register
0x002C	CMU_LCDCLK	LCDCLK Control Register
0x0030	CMU_SEGLCDCLK	SEGLCDCLK Control Register
0x0034	CMU_FMCLK	FMCLK Control Register
0x0038	CMU_PWM0CLK	PWMCLK0 Control Register
0x003C	CMU_PWM1CLK	PWMCLK1 Control Register
0x0040	CMU_PWM2CLK	PWMCLK2 Control Register

0x0044	CMU_PWM3CLK	PWMCLK3 Control Register
0x0048	CMU_PWM4CLK	PWMCLK4 Control Register
0x004C	CMU_PWM5CLK	PWMCLK5 Control Register
0x0050	CMU_PWM6CLK	PWMCLK6 Control Register
0x0054	CMU_PWM7CLK	PWMCLK7 Control Register
0x0058	CMU_PWM8CLK	PWMCLK8 Control Register
0x005C	CMU_LRADCCLK	LRADC CLK Control Register
0x0060	CMU_TIMERCLK	TIMER Clock Control Register
0x0080	CMU_MEMCLKEN	MEMCLKEN Control Register
0x0088	CMU_MEMCLKSEL	MEMCLKSEL Control Register
0x00B0	CMU_DSP_WAIT	DSP Wait Control Register
0x00C0	CMU_DSP_AUDIO_VOLCLK_SEL	DSP Audio Volume Control Register

8.3.3 CMU Digital Register Description

8.3.3.1 CMU_SYSCLK

CMU_SYSCLK Control register, offset = 0x00

Bit (s)	Name	Description	Access	Reset
31:22	-	Reserved	R	0x0
21:20	MEMCLKDIV	MEM_CLK divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
19:18	-	Reserved	R	0x0
17:16	DSPAPBCLKDIV	DSP_APB_CLK divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
15:13	-	Reserved	R	0x0
12	AHBCLKDIV	SCLK divisor 0: /2 1: /4	R/W	0x0
11:8	CPUCLKDIV	CPU_CLK coefficient 0x 0: 1/16 0x 1: 2/16 0x 2: 3/16 0x 3: 4/16 0x 4: 5/16 0x 5: 6/16 0x 6: 7/16 0x 7: 8/16 0x 8: 9/16 0x9: 10/16 0xa: 11/16 0xb: 12/16 0xc: 13/16 0xd: 14/16 0xe: 15/16 0xf: 16/16	R/W	0xf

7:6	-	Reserved	R	0x0
5:4	CORECLKDIV	CORE_CLK Divisor 00: /1 01: /2 10: /4 11: /8	R/W	0x0
3	-	Reserved	R	0x0
2:0	CORE_CLKSEL	CORE_CLK select 000: CK32K 001: CK3M 010: CORE_PLL 011: HOSC 100: CK_64M Others: Reserved	R/W	0x1

8.3.3.2 CMU_DEVCLKEN0

CMU_DEVCLKEN0 Control register, offset = 0x04

Bit (s)	Name	Description	Access	Reset
31	-	Reserved	R/W	0x0
30	EXINTCLKEN	External Interrupt clock enable bit 0: disable 1: enable The source clock of external interrupt is CK3M	R/W	0x1
29	SPI2CLKEN	SPI2 controller clock enable bit 0: disable 1: enable	R/W	0x0
28	I2SSRDCLKEN	I2S Sample Rate Detect Clock Enable 0: disable 1: enable This bit controls the clock gating of I2SSRD_CLK.	R/W	0x0
27	DMICCLKEN	DMIC clock enable bit 0: disable 1: enable	R/W	0x0
26	IRCLKEN	IR clock enable bit 0: disable 1: enable	R/W	0x0
25	TIMERCLKEN	Timer0/1/2/3 controller clock 0: disable 1: enable This bit controls all the clock gatings of TIMERx_CLK.	R/W	0x0
24	-	Reserved	R	0x0
23	USBCLKEN	USB controller clock enable bit 0: disable 1: enable	R/W	0x0
22	LRADCCLKEN	LRADC Controller clock enable bit 0: disable 1: enable	R/W	0x1
21	PWMCLKEN	PWM clock enable bit 0: disable	R/W	0x0

		1: enable This bit controls all the clock gatings of PWMx.		
20	FMCLKEN	FM clock enable bit 0: disable 1: enable	R/W	0x0
19	SEGLCDCLKEN	Segment LCD clock enable bit 0: disable 1: enable	R/W	0x0
18	LCDCLKEN	LCD controller clock enable bit 0: disable 1: enable	R/W	0x0
17	TWICLKEN	TWI controller clock enable bit 0: disable 1: enable	R/W	0x0
16	UART1CLKEN	UART1 controller clock enable bit 0: disable 1: enable	R/W	0x0
15	UART0CLKEN	UART0 controller clock enable bit 0: disable 1: enable	R/W	0x0
14	SPI1DCACHECLKEN	SPI1DCACHE Controller clock enable bit 0: disable 1: enable	R/W	0x0
13	SPI0CACHECLKEN	SPICACHE Controller clock enable bit 0: disable 1: enable	R/W	0x0
12	SPI1CLKEN	SPI1 controller clock enable bit 0: disable 1: enable	R/W	0x0
11	SPI0CLKEN	SPI0 controller clock enable bit 0: disable 1: enable	R/W	0x0
10	SD1CLKEN	SD1 card controller clock enable bit 0: disable 1: enable	R/W	0x0
9	SD0CLKEN	SD0 card controller clock enable bit 0: disable 1: enable	R/W	0x0
8	SPDIFRXCLKEN	SPDIF RX clock enable bit 0: disable 1: enable This bit will enable the HOSC Clock which is sent to SPDIFRX module detecting Audio Sample Rate.	R/W	0x0
7	SPDIFTXCLKEN	SPDIF TX clock enable bit 0: disable 1: enable	R/W	0x0
6	I2SRX1MCLKEN	I2S1 RX1 Mclock enable bit 0: disable 1: enable	R/W	0x0
5	I2SRX0MCLKEN	I2S RX0 Mclock enable bit 0: disable	R/W	0x0

		1: enable		
4	I2STXMCLKEN	I2S TX Mclock enable bit 0: disable 1: enable	R/W	0x0
3	ADCCLKEN	ADC controller clock enable bit 0: disable 1: enable	R/W	0x0
2	DACCLKEN	DAC controller clock enable bit 0: disable 1: enable	R/W	0x0
1	-	Reserved	R	0x0
0	DMACLKEN	DMA clock enable bit 0: disable 1: enable	R/W	0x0

8.3.3.3 CMU_DEVCLKEN1

CMU_DEVCLKEN1 Control register, offset = 0x08

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R/W	0x0
29	DSPCLKEN	DSP clock(DSP_CLK, DSP_APB_CLK, DSP_AXI_CLK) enable bit 0: disable 1: enable	R/W	0x0
28	DSPCPUREGCLKEN	DSP and CPU Communication Register Clock enable bit 0: disable 1: enable	R/W	0x0
27:0	-	Reserved	R/W	0x0

8.3.3.4 CMU_ADDACLK

CMU_ADDACLK Control register, offset = 0x0014

Bit (s)	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	ADCCLKSRC	ADC_CLK Clock Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
11	ADCCLKPREDIV	ADC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
10:8	ADCCLKDIV	ADC_CLK Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0
7:5	-	Reserved	R	0x0
4	DACCLKSRC	DAC_CLK Clock Source	R/W	0x0

		0: AudioPLL0 1: AudioPLL1		
3	DACCLKPREDIV	DAC_CLK Clock Pre-Divisor 0: /1 1: /2	R/W	0x0
2:0	DACCLKDIV	DAC_CLK Clock Divisor. see note 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0

8.3.3.5 CMU_I2SCLK

CMU_I2SCLK Control register, offset = 0x0018

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R	0x0
29:28	I2SRDCLKSRC	I2S Sample Rate Detect Clock Source 00: AudioPLL0 01: AudioPLL1 10: reserved 11: HOSC	R/W	0x0
27	-	Reserved	R	0x0
26	I2SRX1MCLKEXTREV	I2SRX1_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
25:24	I2SRX1MCLKSRC	I2SRX1_MCLK Source 00: I2S1_CLK 01: I2STX_MCLK 10: I2SRX0_MCLK 11: I2SRX1_MCLK_EXT	R/W	0x0
23:21	-	Reserved	R	0x0
20	I2S1CLKSRC	I2S1_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
19	I2S1CLKPREDIV	I2S1_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
18:16	I2S1CLKDIV	I2S1_CLK Divisor 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0
15	-	Reserved	R	0x0
14	I2SRX0MCLKEXTREV	I2SRX0_MCLK_EXT Reverse 0: Normal	R/W	0x0

		1: Reversed		
13:12	I2SRX0MCLKSRC	I2SRX0_MCLK Source 00: ADC_CLK 01: I2STX_MCLK 10: I2S1_CLK 11: I2SRX0_MCLK_EXT	R/W	0x0
11	I2STXMCLKEXTREV	I2STX_MCLK_EXT Reverse 0: Normal 1: Reversed	R/W	0x0
10	I2STXMCLKDACSRC	I2STX_MCLK DAC Source 0: DAC_256fs_CLK 1: DAC_128fs_CLK	R/W	0x0
9:8	I2STXMCLKSRC	I2STX_MCLK Source 00: DAC_256fs_128fs_CLK (according to bit10) 01: ADC_CLK 10: I2S0_CLK 11: I2STX_MCLK_EXT	R/W	0x0
7:5	-	Reserved	R	0x0
4	I2S0CLKSRC	I2S0_CLK Source 0: AudioPLL0 1: AudioPLL1	R/W	0x0
3	I2S0CLKPREDIV	I2S0_CLK Pre-Divisor 0: /1 1: /2	R/W	0x0
2:0	I2S0CLKDIV	I2S0_CLK Divisor 000: /1 001: /2 010: /3 011: /4 100: /6 101: /8 110: /12 111: ----	R/W	0x0

8.3.3.6 CMU_SPDIFCLK

CMU_SPDIFCLK Control register, offset = 0x001C

Bit (s)	Name	Description	Access	Reset
31:6	-	Reserved	R	0x0
5:4	SPDIFTXCLKSRC	SPDIFTX_CLK Source 00: DAC_128fs_CLK 01: I2S0_CLK 10: I2S0_CLK/2 11: Reserved	R/W	0x0
3:2	SPDIFRXCLKSRC	SPDIFRX_CLK Source 00: AudioPLL0 01: AudioPLL1 10: CorePLL 11: Reserved	R/W	0x0
1:0	SPDIFRXCLKDIV	SPDIFRX_CLK Divisor 0: /1 1: 2/3 2: /2	R/W	0x0

		3: /3		

8.3.3.7 CMU_SDCLK

CMU_SDCLK Control register, offset = 0x0020

Bit (s)	Name	Description	Access	Reset
31:15	-	Reserved	R	0x0
14	SD1CLKSRC	SD1 Card Controller Clock Source Select 0: HOSC 1: CORE_PLL	R/W	0x0
13	-	Reserved	R	0x0
12	SD1CLKPOSTDIV	SD1 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
11:8	SD1CLKDIV	SD1 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13 1101: /14 1110: /15 1111: /16	R/W	0x0
7	-	Reserved	R	0x0
6	SD0CLKSRC	SD0 Card Controller Clock Source Select 0: HOSC 1: CORE_PLL	R/W	0x0
5	-	Reserved	R	0x0
4	SD0CLKPOSTDIV	SD0 Card Controller Clock Post-Divisor 0: /1 1: /128	R/W	0x0
3:0	SD0CLKDIV	SD0 Card Controller Clock Divisor 0000: /1 0001: /2 0010: /3 0011: /4 0100: /5 0101: /6 0110: /7 0111: /8 1000: /9 1001: /10 1010: /11 1011: /12 1100: /13	R/W	0x0

		1101: /14 1110: /15 1111: /16		

8.3.3.8 CMU_SPICLK

CMU_SPICLK Control register, offset = 0x0024

Bit (s)	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23:22	SPI2CLKSRC	SPI2 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
21	-	Reserved	R	0x0
20:16	SPI2CLKDIV	SPI2 Clock Divisor 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0
15:14	SPI1CLKSRC	SPI1 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
13	-	Reserved	R	0x0
12:8	SPI1CLKDIV	SPI1 Clock Divisor 0: /1 1: /2 2: /3 3: /4 4: /5 … 29: /30 30: /1.5 31: /2.5	R/W	0x0
7:6	SPI0CLKSRC	SPI0 Controller Clock Source 00: SCLK 01: HOSC 10: CORE_PLL 11: CK_64M	R/W	0x0
5	-	Reserved	R	0x0
4:0	SPI0CLKDIV	SPI0 Clock Divisor 0: /1 1: /2 2: /3 3: /4 4: /5	R/W	0x0

		... 29: /30 30: /1.5 31: /2.5		

8.3.3.9 CMU_IRCLK

CMU_IRCLK Control register, offset = 0x0028

Bit (s)	Name	Description	Access	Reset
31:1	-	Reserved	R	0x0
0	IRCLKSRC	IR Controller Clock Source 0: HOSC/120 1: CK200K	R/W	0x0

8.3.3.10 CMU_LCDCLK

CMU_LCDCLK Control register, offset = 0x002C

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	LCDCLKSRC	LCD Controller Clock Source 0: HOSC 1: CORE_PLL	R/W	0x0
3	-	Reserved	R	0x0
2:0	LCDCLKDIV	LCD Controller Clock Divisor 000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: Reserved	R/W	0x0

8.3.3.11 CMU_SEGLCDCLK

CMU_SEGLCDCLK Control register, offset = 0x0030

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	SEGLCDCLKSRC	SEGLCD Controller Clock Source 0: CK32K 1: HOSC	R/W	0x0
3	SEGLCDCLKPOSTDIV	SEGLCD Controller Clock Post-Divisor 0: /1 1: /512	R/W	0x0
2:0	SEGLCDCLKDIV	SEGLCD Controller Clock Divisor 000: /1 001: /2 010: /3 011: /4 100: /5 101: /8 110: /16	R/W	0x0

		111: /32		

8.3.3.12 CMU_FMCLK

CMU_FMCLK Control register, offset = 0x0034

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1:0	FMCLKSEL	FM Clock Source 00: HOSC/2 01: HOSC 10: CORE_PLL/10 11: Reserved	R/W	0x0

8.3.3.13 CMU_PWM0CLK

CMU_PWM0CLK Control register, offset = 0x0038

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM0CLKSRC	PWM0 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM0CLKDIV	PWM0 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.14 CMU_PWM1CLK

CMU_PWM1CLK Control register, offset = 0x003C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM1CLKSRC	PWM1 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM1CLKDIV	PWM1 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096	R/W	0x0

		260: /8192 261~511: reserved		

8.3.3.15 CMU_PWM2CLK

CMU_PWM2CLK Control register, offset = 0x0040

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM2CLKSRC	PWM2 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM2CLKDIV	PWM2 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.16 CMU_PWM3CLK

CMU_PWM3CLK Control register, offset = 0x0044

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM3CLKSRC	PWM3 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM3CLKDIV	PWM3 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.17 CMU_PWM4CLK

CMU_PWM4CLK Control register, offset = 0x0048

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM4CLKSRC	PWM4 Controller Clock Source 00: CK32K	R/W	0x0

		01: HOSC 10/11: CK64M		
8:0	PWM4CLKDIV	PWM4 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.18 CMU_PWM5CLK

CMU_PWM5CLK Control register
Offset = 0x004C

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM5CLKSRC	PWM5 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM5CLKDIV	PWM5 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.19 CMU_PWM6CLK

CMU_PWM6CLK Control register, offset = 0x0050

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM6CLKSRC	PWM6 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM6CLKDIV	PWM6 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048	R/W	0x0

		259: /4096 260: /8192 261~511: reserved		

8.3.3.20 CMU_PWM7CLK

CMU_PWM7CLK Control register, offset = 0x0054

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM7CLKSRC	PWM7 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM7CLKDIV	PWM7 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.21 CMU_PWM8CLK

CMU_PWM8CLK Control register, offset = 0x0058

Bit (s)	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10:9	PWM8CLKSRC	PWM8 Controller Clock Source 00: CK32K 01: HOSC 10/11: CK64M	R/W	0x0
8:0	PWM8CLKDIV	PWM8 Controller Clock Divisor 0: /1 1: /2 … 255: /256 256: /512 257: /1024 258: /2048 259: /4096 260: /8192 261~511: reserved	R/W	0x0

8.3.3.22 CMU_LRADCCLK

CMU_LRADCCLK Control register, offset = 0x005C

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1:0	LRADCCLKSRC	LRADC Clock Source	R/W	0x0

		00: HOSC/94 255KHz 01: HOSC/47 511KHz 10: HOSC/23 1043KHz 11: CK3M/12 250KHz		

8.3.3.23 CMU_TIMERCLK

CMU_TIMERCLK Control register, offset = 0x0060

Bit (s)	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:6	TIMER3CLKSRC	Timer3 clock Source 0: HOSC 1: HOSC/24 2: TIMER3_EXT 3: Reserved	R/W	0x0
5:4	TIMER2CLKSRC	Timer2 clock Source 0: HOSC 1: HOSC/24 2: TIMER2_EXT 3: Reserved	R/W	0x0
3:2	TIMER1CLKSRC	Timer1 clock Source 0: HOSC 1: HOSC/24 Others: Reserved	R/W	0x0
1:0	TIMER0CLKSRC	Timer0 clock Source 0: HOSC 1: HOSC/24 Others: Reserved	R/W	0x0

8.3.3.24 CMU_MEMCLKEN

CMU_MEMCLKEN Control register, offset = 0x0080

Bit (s)	Name	Description	Access	Reset
31:29	-	Reserved	R	0x0
28	SPI1DCACHERAMCLKEN	SPI1 cache RAM clock enable bit 0: disable 1: enable	R/W	0x1
27	URAM2CLKEN	URAM2 clock enable bit 0: disable 1: enable	R/W	0x1
26	-	Reserved	R	0x0
25	URAM1CLKEN	URAM1 clock enable bit 0: disable 1: enable	R/W	0x1
24	-	Reserved	R	0x0
23	URAM0CLKEN	URAM0 clock enable bit 0: disable 1: enable	R/W	0x1
22	SD1BUFCLKEN	SD1BUF0/1 clock enable bit 0: disable 1: enable	R/W	0x1
21	SD0BUFCLKEN	SD0BUF0/1 clock enable bit	R/W	0x1

		0: disable 1: enable		
20:19	-	Reserved	R/W	0x1
18	PCMRAM6CLKEN	PCMRAM6 clock enable bit 0: disable 1: enable	R/W	0x1
17	PCMRAM5CLKEN	PCMRAM5 clock enable bit 0: disable 1: enable	R/W	0x1
16	PCMRAM4CLKEN	PCMRAM4 clock enable bit 0: disable 1: enable	R/W	0x1
15	PCMRAM3CLKEN	PCMRAM3 clock enable bit 0: disable 1: enable	R/W	0x1
14	PCMRAM2CLKEN	PCMRAM2 clock enable bit 0: disable 1: enable	R/W	0x1
13	PCMRAM1CLKEN	PCMRAM1 clock enable bit 0: disable 1: enable	R/W	0x1
12	PCMRAM0CLKEN	PCMRAM0 clock enable bit 0: disable 1: enable	R/W	0x1
11	RAMFUNCLKEN	CPU Access RAM Function clock enable bit 0: disable 1: enable Once this bit is cleared, the clock for CPU accessing the above RAM such as PCMRAM0, URAM0, willed be gated, so that the related circuit will turned off to save more power	R/W	0x1
10:9	-	Reserved	R	0x0
8	RAM7CLKEN	RAM7 clock enable bit 0: disable 1: enable	R/W	0x1
7	RAM6CLKEN	RAM6 clock enable bit 0: disable 1: enable	R/W	0x1
6	RAM5CLKEN	RAM5 clock enable bit 0: disable 1: enable	R/W	0x1
5	RAM4CLKEN	RAM4 clock enable bit 0: disable 1: enable	R/W	0x1
4	RAM3CLKEN	RAM3 clock enable bit 0: disable 1: enable	R/W	0x1
3	RAM2CLKEN	RAM2 clock enable bit 0: disable 1: enable	R/W	0x1
2	RAM1CLKEN	RAM1 clock enable bit 0: disable	R/W	0x1

		1: enable		
1	RAM0CLKEN	RAM0 clock enable bit 0: disable 1: enable	R/W	0x1
0	ROMRAMCLKEN	ROM0~5 clock enable bit 0: disable 1: enable	R/W	0x1

8.3.3.25 CMU_MEMCLKEN1

CMU_MEMCLKEN1 Control register, offset = 0x0084

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	R	0x0
3	RAM11CLKEN	RAM11 clock enable bit 0: disable 1: enable	R/W	0x1
2	RAM10CLKEN	RAM10 clock enable bit 0: disable 1: enable	R/W	0x1
1	RAM9CLKEN	RAM9 clock enable bit 0: disable 1: enable	R/W	0x1
0	RAM8CLKEN	RAM0 clock enable bit 0: disable 1: enable	R/W	0x1

8.3.3.26 CMU_MEMCLKSEL

CMU_MEMCLKSEL Control register, offset = 0x0088

Bit (s)	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27	URAM2CLKSEL	URAM1 clock selection bit 0: CPU_CLK 1: USBctl_URAM_CLK	R/W	0x0
26:25	URAM1CLKSEL	URAM1 clock selection bit 00: CPU_CLK 01: USBctl_URAM_CLK Others: Reserved	R/W	0x0
24:23	URAM0CLKSEL	URAM0 clock selection bit 00: CPU_CLK 01: USBctl_URAM_CLK Others: Reserved	R/W	0x0
22	SD1BUFCLKSEL	SD1BUF0/1 clock selection bit 0: CPU_CLK 1: CARD_MEM_CLK0/1	R/W	0x0
21	SD0BUFCLKSEL	SD0BUF0/1 clock selection bit 0: CPU_CLK 1: CARD_MEM_CLK0/1	R/W	0x0
20:0			R/W	0x0

8.3.3.27 CMU_DSP_WAIT

DSP Wait Control Register, offset＝0x00B0

Bit (s)	Name	Description	Access	Reset
31	DSPWEN	DSP Wait enable 0: disable 1: enable	R/W	0x0
30:5	-	Reserved	R	0x0
4	DSP_IDLE_CLKEN	DSP Idle Status Clock Gating Enable 0: disable: DSPCLK is on 1: enable: when idled DSPCLK is off. When set to 1, only if DSP idle(PSU_DSP_IDLE) is high, then the DSPCLK and DSPAPBCLK is gated. When cleared, the DSPCLK and DSPAPBCLK is on.	R/W	0x0
3	PSU_DSP_IDLE	DSP Status Indication 0: active status 1: idle status Note: after the PSU_DSP_IDLE becomes '1', the user can externally shut down the DSP root clock(gated by CMU).	R	0x0
2	PSU_DSP_COREIDLE	DSP Core Status Indication 0: active status 1: idle status Note: when the PSU_DSP_COREIDLE becomes '1', only the DSP Internal core clock is gated.	R	0x0
1	DSP_WAIT_AFTER_MPU	DSP Wait or not after DSP MPU Interrupt 0: no wait 1: wait	R/W	0x0
0	DSPDEWS	DSP external wait signal 0: no force wait 1: force wait	R/W	0x0

8.3.3.28 CMU_DSP_AUDIO_VOLCLK_SEL

DSP Audio Volume Control Register, offset = 0x00C0

Bit (s)	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	PAVOL_CLK_SEL	Audio PA_VOLUME register clock select 0: SCLK 1: DSP_CLK	R/W	0x0
1	LCHVOL_CLK_SEL	Audio VOL_LCH register clock select 0: SCLK 1: DSP_CLK	R/W	0x0
0	RCHVOL_CLK_SEL	Audio VOL_RCH register clock select 0: SCLK 1: DSP_CLK	R/W	0x0

8.4 RTC

This part have individual modules: Calendar, Watch Dog (WD) and Timer0/1/2/3.

8.4.1 Features

- Calendar with a alarm IRQ which can wake up the PMU
- Four Timers with IRQS, while two as universal timer and two timer had get capture timer
- A watch dog which can be configured optional as IRQ or Reset

8.4.2 RTC Register List

Table 8-7 RTC block base address

Name	Physical Base Address	KSEG1 Base Address
RTC	0xC0120000	0xC0120000

Table 8-8 RTC Controller Registers

Offset	Register Name	Description
0x0000	RTC_CTL	RTC Control Register
0x0008	RTC_DHMSALM	RTC Day Hour Minute and Second Alarm Register
0x000C	RTC_DHMS	RTC Day Hour Minute and Second Register
0x0010	RTC_YMD	RTC Year Month Date Register
0x0014	RTC_ACCESS	RTC freely access Register
0x001C	WD_CTL	Watch Dog Control register

8.4.3 RTC Register Description

8.4.3.1 RTC_CTL

Calendar Control Register, offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	LEAP	RTC Leap Year bit 0: not leap year 1: leap year	R	0x1
6:5	-	Reserved	R	0x0
4	CAL_EN	Calendar Enable 0: Disable 1: Enable	R/W	0x0
3:2	CALENDAR_CLK_SEL	00: select HCL division 01: Build-in OSC 11: Build-in OSC 10: select HOSC division	R/W	0x0
1	ALIE	Alarm IRQ Enable 0: Disable 1: Enable	R/W	0x0
0	ALIP	Alarm IRQ Pending bit, Writing ‘1’ to this bit will clear it.	R/W	0x0

8.4.3.2 RTC_DHMSALM

Offset=0x0008

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0x0
20:16	HOUEAL	Alarm hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MINAL	Alarm minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SECAL	Alarm second setting 00H – 3BH	R/W	0x0

8.4.3.3 RTC_DHMS

Offset=0x000C

Bits	Name	Description	Access	Reset
31:21	-	Reserved	R	0x0
20:16	HOUR	Time hour setting 00H – 17H	R/W	0x0
15:14	-	Reserved	R	0x0
13:8	MIN	Time minute setting 00H – 3BH	R/W	0x0
7:6	-	Reserved	R	0x0
5:0	SEC	Time second setting 00H – 3BH	R/W	0x0

8.4.3.4 RTC_YMD

Offset=0x0010

Bits	Name	Description	Access	Reset
31:23	-	Reserved	R	0x0
22:16	YEAR	Time year setting 00H – 63H	R/W	0x0
15:12	-	Reserved	R	0x0
11:8	MON	Time month setting 01H – 0CH	R/W	0x1
7:5	-	Reserved	R	0x0
4:0	DATE	Time day setting 01H – 1FH	R/W	0x1

8.4.3.5 RTC_ACCESS

Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	ACCESS	These bits can be accessed by CPU freely.	R/W	0x0

8.4.3.6 WD_CTL

Offset=0x001C

Bits	Name	Description	Access	Reset
31	EJTAG_F	CAN READ AND WRITE FREELY	R/W	0x0

30:7	-	reserved	R	0x0
6	IRQP	Watch dog IRQ pending bit; Writing '1' to this bit will clear it.	R/W	0x0
5	SIGS	Watchdog Signal (IRQ or Reset) Select 0: Send Reset signal when watchdog overflow 1: Send IRQ signal when watchdog overflow	R/W	0x0
4	WDEN	Watch Dog timer enable, when WD timer is enabled and the WD timer overflows, an internal reset (WDRST-) is generated to force the system into reset status and then reboot. 0: Disable 1: Enable	R/W	0x0
3:1	CLKSEL	Watch Dog timer Clock Select, The watch dog's overflow value is 180. 000 1khz 176ms 001 512hz 352ms 010 256hz 703ms 011 128hz 1.4s 100 64hz 2.8s 101 32hz 5.6s 110 16hz 11.2s 111 10ms	R/W	0x0
0	CLR	Clear bit, Writing '1' to clear WD timer automatically.	R/W	0x0

8.4.4 TIMER Register List

Table 8-9 TIMER block base address

Name	Physical Base Address	KSEG1 Base Address
TIMER_REGISTER	0xC0120100	0xC0120100

Table 8-10 TIMER Controller Registers

Offset	Register Name	Description
0x00	T0_CTL	Timer0 Control register
0x04	T0_VAL	Timer0 Value
0x08	T0_CNT	Timer0 current counter register
0x20	T1_CTL	Timer1 Control register
0x24	T1_VAL	Timer1 Value
0x28	T1_CNT	Timer1 current counter register
0x40	T2_CTL	Timer2 Control register
0x44	T2_VAL	Timer2 Value
0x48	T2_CNT	Timer2 current counter register
0x4c	T2_CAP	Timer2 capture value register
0x60	T3_CTL	Timer3 Control register
0x64	T3_VAL	Timer3 Value
0x68	T3_CNT	Timer3 current counter register
0x6c	T3_CAP	Timer3 capture value register

8.4.5 TIMER Register Description

8.4.5.1 T0_CTL

Timer0 control register, offset=0x0000

Bits	Name	Description	Access	Reset
31:6	-	reserved	R	0x0
5	EN	Timer 0 Enable 0: Disable 1: Enable	R/W	0x0
4:3	-	Reserved	R	0x0
2	RELO	Timer 0 Reload 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer0 IRQ Enable When this bit is enabled, Timer0_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer0 IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.2 T0_VAL

Timer0 value register, offset=0x0004

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write Timer/Counter value register Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.3 T0_CNT

Timer0 current counter register, offset=0x0008

Bits	Name	Description	Access	Reset
31:0	CNT	Read or write current Timer0 value	R	0x0

8.4.5.4 T1_CTL

Timer1 control register, offset=0x0020

Bits	Name	Description	Access	Reset
31:6	-	reserved	R	0x0
5	EN	Timer 1 Enable 0: Disable 1: Enable	R/W	0x0
4:3	-	Reserved	R	0x0
2	RELO	Timer 1 Reload 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer1 IRQ Enable When this bit is enabled, Timer1_Zero_IRQ sent out the IRQ signal until the pending bit was cleared.	R/W	0x0
0	ZIPD	Timer1 IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.5 T1_VAL

Timer1 value register, offset=0x0024

Bits	Name	Description	Access	Reset
31:0	VAL	Read or write current Timer1 value Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.6 T1_CNT

Timer1 current counter register, offset=0x0028

Bits	Name	Description	Access	Reset
31:0	CNT	Read or write current Timer1 value	R	0x0

8.4.5.7 T2_CTL

Timer2 control register, offset=0x0040

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	LEVEL	Current input pulse level Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set 0: down 1: up	R/W	0x0
10:9	MODE_SEL	Timer mode select 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Capture event IRQ pending; Writing ‘1’ to clear this bit. IRQ pending include counter mode and capture mode.	R/W	0x0
7:6	CAPTURE_SE	Capture signal edge select 00: falling edge 01: rising edge 1x: both falling edge and rising edge Edge select include counter mode and capture mode.	R/W	0x0
5	EN	Timer2 Enable 0: Disable 1: Enable	R/W	0x0
4:3	-	reserved	R	0x0
2	RELO	Timer2 Reload enable 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer2 IRQ Enable When this bit is enabled, Timer2_IRQ sent out the IRQ signal until the pending bit was cleared. If DIR=’0’, T2_CNT compare with ZERO. If DIR=’1’, T2_CNT compare with T2_VAL. In input capture mode, every trigger edge would cause a capture IRQ, which pending reference to CAPTURE_IP.	R/W	0x0
0	ZIPD	Timer2 IRQ Pending; Writing ‘1’ to clear this bit. If timer overflow or zero occurs, this pending would be set to ‘1’.	R/W	0x0

8.4.5.8 T2_VAL

Timer2 value register, offset=0x0044

Bits	Name	Description	Access	Reset

31:0	VAL	Set timer counter value If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an IRQ. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an IRQ. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. In counter mode, Tx_VAL[7:0] was used. Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.9 T2_CNT

Timer2 current counter register, offset=0x0048

Bits	Name	Description	Access	Reset
31:0	CNT	Timer current value registers	R	0x0

8.4.5.10 T2_CAP

Timer2 current counter register, offset=0x004C

Bits	Name	Description	Access	Reset
31:0	CAP	Capture value register Using in capture mode, when capture IRQ occurred, read this register to get counter of pulse width counter. If would be reload by every trigger edge set in Tx_CTL.	R	0x0

8.4.5.11 T3_CTL

Timer3 control register, offset=0x0060

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	LEVEL	Current input pulse level Using for counter mode and capture mode	R	0x0
11	DIR	Timer Counting direction set 0: down 1: up	R/W	0x0
10:9	MODE_SEL	Timer mode select 00 : normal timer 01 : counter mode 10 : input capture mode 11 : reserved	R/W	0x0
8	CAPTURE_IP	Capture event IRQ pending; Writing ‘1’ to clear this bit. IRQ pending include counter mode and capture mode.	R/W	0x0
7:6	CAPTURE_SE	Capture signal edge select 00: falling edge 01: rising edge 1x: both falling edge and rising edge Edge select include counter mode and capture mode.	R/W	0x0
5	EN	Timer3 Enable 0: Disable 1: Enable	R/W	0x0

4:3	-	reserved	R	0x0
2	RELO	Timer3 Reload enable 0: Not reload 1: Reload	R/W	0x0
1	ZIEN	Timer IRQ Enable In timer/counter mode, When this bit is enabled, Timer3_Zero_IRQ sent out the IRQ signal until the pending bit was cleared. If DIR='0', T3_CNT compare with ZERO. If DIR='1', T3_CNT compare with T3_VAL. In input capture mode, every trigger edge would cause a capture IRQ, which pending reference to CAPTURE_IP.	R/W	0x0
0	ZIPD	Timer3 mode IRQ Pending; Writing '1' to clear this bit.	R/W	0x0

8.4.5.12 T3_VAL

Timer3 value register, offset=0x0064

Bits	Name	Description	Access	Reset
31:0	VAL	Set timer counter value. If timer setting in count up mode, time would count up from zero to the value set in Tx_VAL. when the current timer counter equal to Tx_VAL, it would cause an IRQ. If timer reload mode was set, Tx_VAL would be reload auto and timer current value was reset to zero. If timer setting in countdown mode, timer would countdown form Tx_VAL to zero. When the current timer counter equal to zero. it would cause an IRQ. If timer reload mode was set, zero would be reload auto and timer current value was reset to Tx_VAL. In counter mode, Tx_VAL[7:0] was used. Note: If set Tx_VAL=n, IRQ would cause after n+1 Tx_CLK.	R/W	0x0

8.4.5.13 T3_CNT

Timer3 current counter register, offset=0x0068

Bits	Name	Description	Access	Reset
31:0	CNT	Timer current value registers	R	0x0

8.4.5.14 T3_CAP

Timer3 current counter register, offset=0x006C

Bits	Name	Description	Access	Reset
31:0	CAP	Capture value register Using in capture mode, when capture IRQ occurred, read this register to get counter of pulse width counter.	R	0x0

8.5 Exceptions and Interrupts Controller (INTC)

8.5.1 INTC Register List

Table 8-11 Interrupt Controller base address

Name	Physical Base Address	KSEG1 Base Address
Interrupt_Controller	0xC00B0000	0xC00B0000

Table 8-12 Interrupt Controller Registers

Offset	Register Name	Description
0x00000028	REQ_INT_OUT	Request interrupt output register
0x0000002C	REQ_IN	Request input register
0x00000030	REQ_IN_PD	Request input pending register
0x00000034	REQ_OUT	Request output register
0x00000040	CPU_WAKEUP_EN0	Interrupt Source Wakeup CPU enable register 0
0x00000044	CPU_WAKEUP_EN1	Interrupt Source Wakeup CPU enable register 1
0x00000050	CPU_DSP_INT_EN	CPU to DSP Interrupt enable register

8.5.2 INTC Register Description

8.5.2.1 REQ_INT_OUT

Request interrupt output register, offset = 0x00000028

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1	DSP_INT1	Send interrupt request to DSP INT1.	R/W	0x0
0	DSP_INT0	Send interrupt request to DSP INT0.	R/W	0x0

8.5.2.2 REQ_IN

Request input register, offset = 0x0000002C

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	OUT_USER4	It is a CPU interrupt controller sampled value of OUT_USER4 signal.	R	0x0
3	OUT_USER3	It is a CPU interrupt controller sampled value of OUT_USER3 signal.	R	0x0
2	OUT_USER2	It is a CPU interrupt controller sampled value of OUT_USER2 signal.	R	0x0
1	OUT_USER1	It is a CPU interrupt controller sampled value of OUT_USER1 signal.	R	0x0
0	OUT_USER0	It is a CPU interrupt controller sampled value of OUT_USER0 signal.	R	0x0

Note: 0: Interrupt is masked. 1: Interrupt is unmasked.

8.5.2.3 REQ_IN_PD

Request input pending register, offset = 0x00000030

Bit (s)	Name	Description	Access	Reset
31:5	-	Reserved	R	0x0
4	OUT_USER4_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER4 signal. Writing '1' can clear this bit.	R/W	0x0

3	OUT_USER3_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER3 signal. Writing '1' can clear this bit.	R/W	0x0
2	OUT_USER2_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER2 signal. Writing '1' can clear this bit.	R/W	0x0
1	OUT_USER1_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER1 signal. Writing '1' can clear this bit.	R/W	0x0
0	OUT_USER0_PD	0: interrupt pending is not detected. 1: interrupt pending is detected. External Interrupt Pending is set at rising edge of DSP OUT_USER0 signal. Writing '1' can clear this bit.	R/W	0x0

8.5.2.4 REQ_OUT

Request output register, offset = 0x00000034

Bit (s)	Name	Description	Access	Reset
31:2	-	Reserved	R	0x0
1	IN_USER1	Send information to DSP(INT0/INT1).	R/W	0x0
0	IN_USER0	Send information to DSP(INT0/INT1).	R/W	0x0

8.5.2.5 CPU_WAKEUP_EN0

Interrupt Source Wakeup CPU enable register, offset = 0x00000040

Bit (s)	Name	Description	Access	Reset
31:30	-	Reserved	R	0x0
29	DMA7_WAKEUP_EN	DMA7 wake up source enable bit 0: disable 1: enable	R/W	0x0
28	DMA6_WAKEUP_EN	DMA6 wake up source enable bit 0: disable 1: enable	R/W	0x0
27	DMA5_WAKEUP_EN	DMA5 wake up source enable bit 0: disable 1: enable	R/W	0x0
26	DMA4_WAKEUP_EN	DMA4 wake up source enable bit 0: disable 1: enable	R/W	0x0
25	DMA3_WAKEUP_EN	DMA3 wake up source enable bit 0: disable 1: enable	R/W	0x0
24	DMA2_WAKEUP_EN	DMA2 wake up source enable bit 0: disable 1: enable	R/W	0x0
23	DMA1_WAKEUP_EN	DMA1 wake up source enable bit 0: disable 1: enable	R/W	0x0
22	DMA0_WAKEUP_EN	DMA0 wake up source enable bit	R/W	0x0

		0: disable 1: enable		
21	SD1_WAKEUP_EN	SD1 wake up source enable bit 0: disable 1: enable	R/W	0x0
20	SD0_WAKEUP_EN	SD0 wake up source enable bit 0: disable 1: enable	R/W	0x0
19	MPU_WAKEUP_EN	MPU wake up source enable bit 0: disable 1: enable	R/W	0x0
18	I2S1_SPDIF_RX_WAKEUP_EN	I2S1/SPDIF RX wake up source enable bit 0: disable 1: enable	R/W	0x0
17	ADC_I2S_RX_WAKEUP_EN	ADC/I2S RX wake up source enable bit 0: disable 1: enable	R/W	0x0
16	DAC_WAKEUP_EN	DAC wake up source enable bit 0: disable 1: enable	R/W	0x0
15	I2S_SPDIF_TX_WAKEUP_EN	I2S/SPDIF TX wake up source enable bit 0: disable 1: enable	R/W	0x0
14	UART1_WAKEUP_EN	UART1 wake up source enable bit 0: disable 1: enable	R/W	0x0
13	UART0_WAKEUP_EN	UART0 wake up source enable bit 0: disable 1: enable	R/W	0x0
12	TWI_WAKEUP_EN	TWI wake up source enable bit 0: disable 1: enable	R/W	0x0
11	USB_WAKEUP_EN	USB wake up source enable bit 0: disable 1: enable	R/W	0x0
10	SPI1_WAKEUP_EN	SPI1 wake up source enable bit 0: disable 1: enable	R/W	0x0
9	SPI0_WAKEUP_EN	SPI0 wake up source enable bit 0: disable 1: enable	R/W	0x0
8	RTC_WAKEUP_EN	RTC wake up source enable bit 0: disable 1: enable	R/W	0x0
7	GPIO_INT_WAKEUP_EN	GPIO wake up source enable bit 0: disable 1: enable	R/W	0x0
6	TIMER3_WAKEUP_EN	Timer3 wake up source enable bit 0: disable 1: enable	R/W	0x0
5	TIMER2_WAKEUP_EN	Timer2 wake up source enable bit 0: disable 1: enable	R/W	0x0

4	TIMER1_WAKEUP_EN	Timer1 wake up source enable bit 0: disable 1: enable	R/W	0x0
3	TIMER0_WAKEUP_EN	Timer0 wake up source enable bit 0: disable 1: enable	R/W	0x0
2	WD_WAKEUP_EN	Watchdog wake up source enable bit 0: disable 1: enable	R/W	0x0
1	NFC_WAKEUP_EN	NFC wake up source enable bit 0: disable 1: enable	R/W	0x0
0	BT_BB_WAKEUP_EN	0: no interrupt to CPU 1: generate interrupt to CPU BT Baseband set this bit to generate interrupt to CPU. CPU will clear this bit when it handle this interrupt.	R/W	0x0

8.5.2.6 CPU_WAKEUP_EN1

Interrupt Source Wakeup CPU enable register, offset = 0x00000044

Bit (s)	Name	Description	Access	Reset
31	CPUCLK_LOWPOWER_EN	Whether CPU clock needs to be turned off after executing wait instruction 0: disable（do not turn off CPU clock） 1: enable（turn off CPU clock）	R/W	0x0
30:12	-	Reserved	R	0x0
11	SPI2_WAKEUP_EN	SPI2 wake up source enable bit 0: disable 1: enable	R/W	0x0
10:6	-	Reserved	R	0x0
5	IR_WAKEUP_EN	IRC wake up source enable bit 0: disable 1: enable	R/W	0x0
4	OUT_USER4_WAKEUP_EN	0: disable 1: enable	R/W	0x0
3	OUT_USER3_WAKEUP_EN	0: disable 1: enable	R/W	0x0
2	OUT_USER2_WAKEUP_EN	0: disable 1: enable	R/W	0x0
1	OUT_USER1_WAKEUP_EN	0: disable 1: enable	R/W	0x0
0	OUT_USER0_WAKEUP_EN	0: disable 1: enable	R/W	0x0

8.5.2.7 CPU_DSP_INT_EN

CPU to DSP Interrupt enable register, offset = 0x00000050

Bit (s)	Name	Description	Access	Reset
31:4	-	Reserved	R	0x0
3	I2STXFIFOINT_EN	I2STX FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x0

2	DACFIFOINT_EN	DAC FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x1
1	I2SRX1FIFOINT_EN	I2SRX1 FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x0
0	ADCFIFOINT_EN	ADC FIFO Interrupt Enable 0: Disable 1: Enable	R/W	0x1

9 Storage

SD/MMC Card Controller Features

- ATS2835P integrates two SD/MMC controller: SD0 and SD1
- Fully compliant with MMC Specification 4.3
- Fully compliant with SD card Specification 2.0
- Integrated Clock Delay Chain Technique to Regulate Card Interface Timing: Latching Delay Chain for input Signal, Output Delay Chain for output signal.
- Integrated Watchdog timeout Counter to report Exception happening.
- Integrated Pull up resistance (value 50Komh) for Data and CMD Line.
- Integrated CRC calculate and check circuit.
- Send continuous clock to support SDIO card.
- Support 3.1V CLK PAD voltage.
- Support 3.1V CMD PAD voltage.
- Support 3.1V DAT PAD voltage.
- Band Width: 25MByte/S
- Maximal SD interface Clock: 50MHz

10 Transfer and Communication

10.1 USB

10.1.1 Features

- Complies with the USB2.0 Specification Revision 1.0a.
- UTMI+ level2 Transceiver Macrocell Interface.
- Supports point-to-point communication with one full-speed or high-speed device in Host mode (no HUB support).
- Supports full-speed or high-speed in peripheral mode.
- Supports 3 IN endpoint and 3 OUT endpoint except endpoint0.
- Supports bulk Isochronous and Interrupt transfer.
- Partially configurable endpoint endpoint type and single, double triple or quad buffering.
- Integrated synchronous RAM as endpoint FIFOs.
- Supports suspend, resume and power managements function.
- Support remote wakeup for device mode.
- Support DMA transfer for endpoint in1 and out2

10.1.2 USB Register List

Table 10-1 USB Controller Registers Address

Name	Physical Base Address	KSEG1 Base Address
USB_CONTROLLER_REGISTERS	0xC0080000	0xC0080000

Table 10-2 USB Controller Registers

Offset	Register Name	Description
0x421	DPDMCTRL	DPDM control register
0x422	LINESTATUS	Line status register

10.1.3 USB Register Description

10.1.3.1 DPDMCTRL

DP DM control register
Offset = 0x421

Bit (s)	Name	Description	Access	Reset
7	-	Reserved	R	0B
6	PLUGIN	This bit Indicated the usb connection status when Linedeten is enable. 1: connect 0: disconnect	R	x
5	-	Reserved	R	0B
4	LSDETEN	Line status detect enable 1：enable 0：disable	R/W	1B
3	DMPUEN	500Kohm DM pull up resistor enable. 1：enable 0：disable	R/W	0B
2	DPPUEN	500Kohm DP pull up resistor enable. 1：enable 0：disable	R/W	0B
1	DMPDDIS	DM pull down disable. 1：disable 0：enable	R/W	0B
0	DPPDDIS	DP pull down disable. 1：disable 0：enable	R/W	0B

10.1.3.2 LINESTATUS

Line status register
Offset = 0x422

Bit (s)	Name	Description	Access	Reset
7:5	-	Reserved	R	0H
4:3	LINESTATE	USB linestate[1:0] Linestate0:DP Linestase1:DM	R	0B
2:1	-	Reserved	R	0H
0	OTGRESET	USB OTG reset. If AOTG is in reset state, this bit will be set, else it will be 0.	R/W	0B

10.2 TWI

10.2.1 Features

- Both master and slave functions supported
- Support standard mode (100kbps) and fast-speed mode (400kpbs)
- Only 7-bit address mode support
- 8 bit x 8 TX FIFO and 8bit x 8 RX FIFO
- Supports general call
- Pull-up resistors are required on both of the TWI signal lines as the TWI drivers are open drain. Typically external 2.2k-Ohm resisters are used to pull the signals up to VCC if not select internal Pull-Up resistor.

10.2.2 Function Description

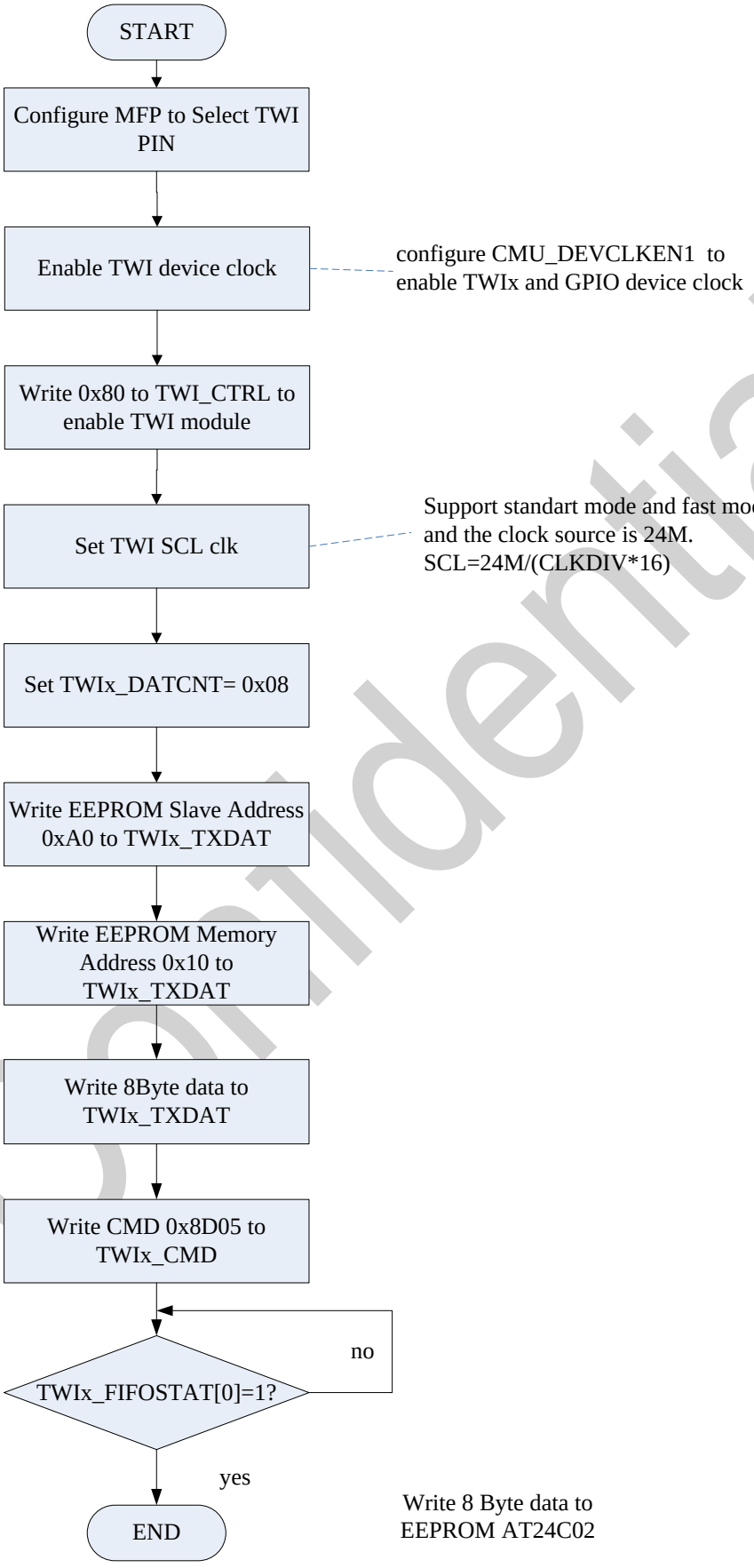
An Inter-IC bus，used to communicate across circuit-board distances. At the low end of the spectrum of communication options for "inside the box" communication is TWI.
TWI provides support for communication with various slow, on-board peripheral devices that are accessed intermittently, while being extremely modest in its hardware resource needs. It is a simple, low-bandwidth, short-distance protocol. Most available TWI devices operate at speeds up to 400Kbit/s, with some venturing up into the low megahertz range. TWI is easy to use to link multiple devices together since it has a built-in addressing scheme.

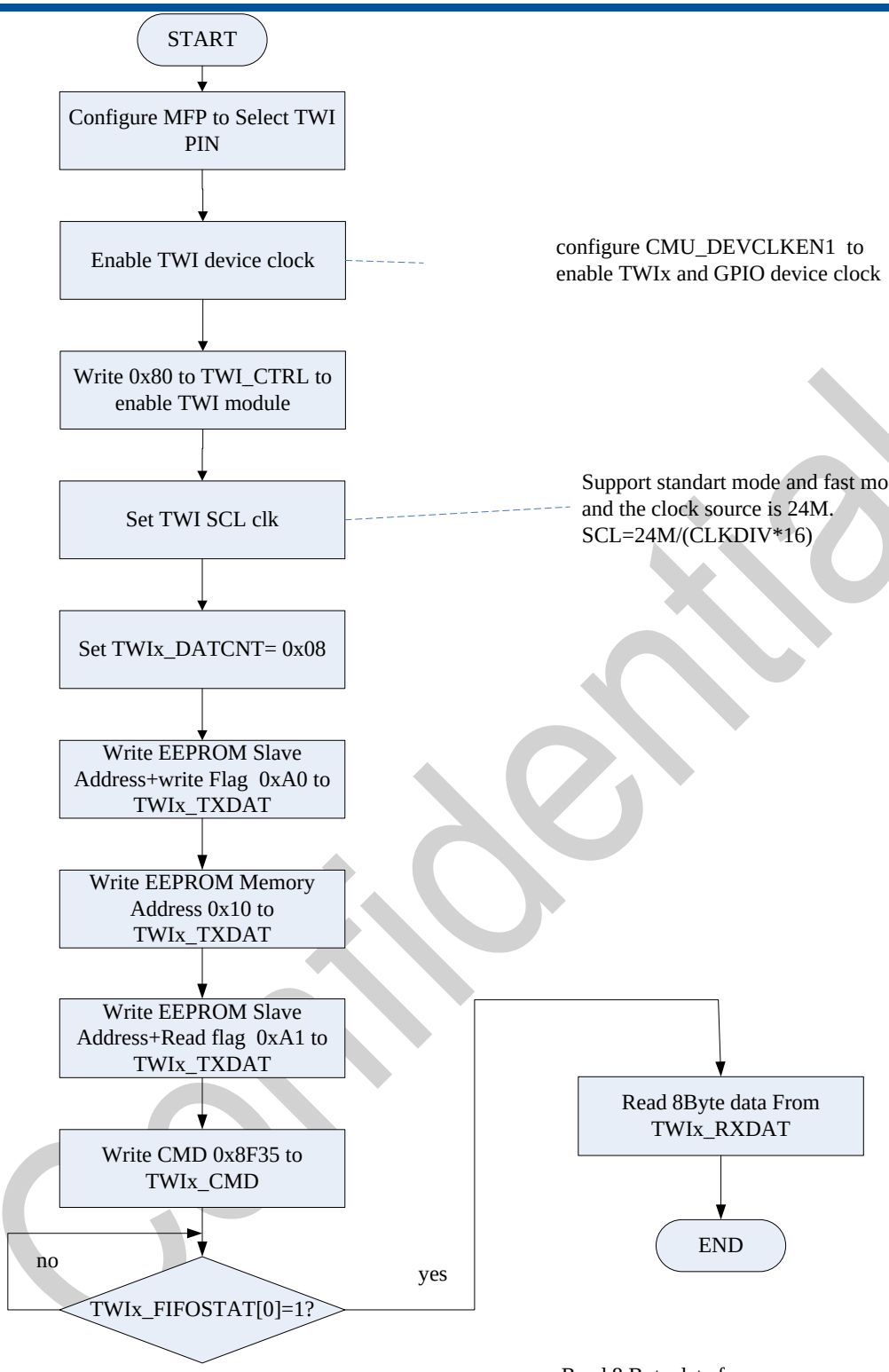
Note:

1. The TWI module is Slave mode when in IDLE status.
2. When write start command, the TWI module change from slave to master mode; and after a stop command change to slave mode.
3. Generate the IRQ while the bus statuses change.
   - transfer complete
   - detect normal stop bit (no bus error)

   If the address received don’t match the content of TWI_address , don’t generate the IRQ and reset to IDLE when detect the start bit followed the slave address in slave mode.
4. Release the bus by software after receive data or address.
5. In multi-master application, when miss the control of the bus, ignore the bus command before a stop command detected. After a stop command, the device start an arbitration procedure. The arbitration will end with one of the following:
   - The TWI module enters master mode (it won the arbitration)
   - The TWI module enters slave mode (it lost the arbitration or the other master addresses the TWI module)
   - The TWI module enter master-in-waiting mode, when the TWI module is waiting for the other master (that won control) to complete its transaction so that it can once again try to grain the arbitration of the bus.

10.2.3 Operation Manual





Read 8 Byte data from EEPROM AT24C02

10.2.4 TWI Register List

Table 10-3 TWI Register Block Base Address

Name	Physical Base Address	KSEG1 Base Address
TWI	0xC0130000	0xC0130000

Table 10-4 TWI Registers Offset Address

Offset	Register Name	Description
0x0000	TWI_CTL	TWI Control Register
0x0004	TWI_CLKDIV	TWI Clock Divider Register
0x0008	TWI_STAT	TWI Status Register
0x000C	TWI_ADDR	TWI Address Register
0x0010	TWI_TXDAT	TWI TX Data Register
0x0014	TWI_RXDAT	TWI RX Data Register
0x0018	TWI_CMD	TWI Command Register
0x001C	TWI_FIFOCTL	TWI FIFO Control Register
0x0020	TWI_FIFOSTAT	TWI FIFO Status Register
0x0024	TWI_DATCNT	TWI Data Transmit Counter Register
0x0028	TWI_RCNT	TWI Data Transmit Remain Counter Register

10.2.5 TWI Register Description

10.2.5.1 TWI_CTL

TWI Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10	IRQC	TWI IRQ Control 0: set when RX FIFO received 1 bytes data in IRQ mode 1: set when RX FIFO received 4 bytes data in IRQ mode	R/W	0x0
9:7	-	Reserved	R	0x0
6	IRQE	IRQ Enable. 0: Disable 1: Enable	R/W	0x0
5	EN	Enable. When enable, reset the status machine to IDLE 0: Disable 1: Enable	R/W	0x0
4	-	Reserved	R/W	0x0
3:2	GBCC	Generating Bus Control Condition (only for master mode). 00: No effect 01: Generating START condition 10: Generating STOP condition 11: Generating Repeated START condition Write the slave address to the TWI_DAT register, select start or restart, and then the start or restart command follow by the slave address will occur on the bus.	R/W	0x0
1	RB	Release Bus. Writing '1' to this bit will release the bus.	R/W	0x0
0	GRAS	Generate ACK or NACK Signal. When receive data 0: generate the ACK signal at 9th clock of SCL 1: generate the NACK signal at 9th clock of SCL	R/W	0x0

10.2.5.2 TWI_CLKDIV

TWI Control Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	CLKDIV	Clock Divider Factor (only for master mode). TWI clock (SCL) can select standard (100kbps) mode and fast (400kbps) mode. Calculating SCL is as following: SCL=24M/(CLKDIV*16)	R/W	0x0

10.2.5.3 TWI_STAT

TWI Status Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:11	-	Reserved	R	0x0
10	SRGC	Slave receive general call 0: not receive a general call 1: receive a general call	R	0x0
9	SAMB	Slave address match bit 0: slave address not match 1: slave address match	R	0x0
8	LBST	Last Byte Status Bit. 0: Indicate the last byte received or transmitted is address 1: Indicate the last byte received or transmitted is data	R	0x0
7	TCB	Transfer complete bit 0: not finish transfer 1: In normal mode: A byte transfer finish, include transfer the ACK or NACK bit Writing '1' to this bit will clear it.	R/W	0x0
6	BBB	Bus busy bit 0: Not busy 1: Busy This bit will set to 1 while the start command detected, and set to 0 after the stop command	R	0x0
5	STAD	Start detect bit, include restart. The bit is clear when the TWI module is disable or when the STOP condition is detected. Writing '1' to the bit will clear it. 0: Start bit is not detected 1: Start bit is detected	R/W	0x0
4	STPD	Stop detect bit The bit is clear when the TWI module is disable or when the START condition is detected. Writing '1' to the bit will clear it. 0: Stop bit is not detected 1: Stop bit is detected	R/W	0x0
3	-	Reserved	R	0x0
2	IRQP	IRQ Pending Bit. 1: IRQ 0: No IRQ Set condition: 1） transfer complete 2） detect normal stop bit (no bus error) 3） arbit fail Clear condition:	R/W	0x0

		Writing '1' to this bit will clear it.		
1	BEB	Bus error bit 0: No error occur 1: Bus error occur Write "1" to clear this bit. The below conditions occur generate error bit: Detect stop bit right after detect start/restart bit. Detect stop, start bit when sending or receiving data.	R/W	0x0
0	RACK	Receive ACK or NACK when transmit data or address 0: NACK 1: ACK The bit will be updated when the 9th of next byte clock arrived	R	0x0

10.2.5.4 TWI_ADDR

TWI Address Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:1	SDAD	Own Slave Device Address. Only use in slave mode. TWI_Addr contains the own address of the module when the device is use in slave mode. Content of the register is irrelevant when the TWI module is functioning as a master.	R/W	0x0
0	-	Reserved	R	0x0

10.2.5.5 TWI_TXDAT

TWI TX Data Register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	DAT	The registers of Data or address to be transfer, or received to. TWIDAT contains the byte to be transmitted on the TWI-bus or a byte that has been received from the TWI-bus. In master mode, along with the data byte to be transmitted, it also includes the slave address. The seven MSB's are the slave TWI device address while the LSB is the Read/Write bit. 8 level FIFO，8 x 8bit	W	0x0

10.2.5.6 TWI_RXDAT

TWI RX Data Register
Offset=0x0014

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	DAT	The Receive data Register 8 level FIFO，8 x 8bit	R	0x0

10.2.5.7 TWI_CMD

TWI Command Register
Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	SECL	Start to execute the command list 0: not execute 1: execute command	R/W	0x0
14:13	-	Reserved	R	0x0
12	WRS	Write or Read select 0: write 1: read This bit only used in Slave mode.	R/W	0x0
11	MSS	Master or slave mode select 0: slave mode 1: Master mode	R/W	0x0
10	SE	Stop enable 0: disable 1: enable	R/W	0x0
9	NS	NACK select 0: not select 1: select generate the NACK signal at 9th clock of SCL of the last byte when read data	R/W	0x0
8	DE	Data enable 0: disable 1: enable The counts of data transmitted depend on the TWIx_CNT register.	R/W	0x0
7:5	SAS	Second address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address	R/W	0x0
4	RBE	Restart bit enable 0: not send restart bit 1: send restart bit	R/W	0x0
3:1	AS	Address select 000: no address 001: 1 byte address 010: 2 byte address 011: 3 byte address 100: 4 byte address 101: 5 byte address 110: 6 byte address 111: 7 byte address The address includes slave address and slave internal memory address.	R/W	0x0

0	SBE	Start bit enable 0: not send start bit 1: send start bit	R/W	0x0

10.2.5.8 TWI_FIFOCTL

TWI FIFO Control Register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:3	-	Reserved	R	0x0
2	TFR	TX FIFO reset bit Writing '1' to reset TX FIFO, auto clear to 0 when Tx FIFO reset complete.	R/W	0x0
1	RFR	RX FIFO reset bit Writing '1' to reset RX FIFO, auto clear to 0 when Rx FIFO reset complete.	R/W	0x0
0	NIB	NACK Ignore Bit 0: not ignore, when receive NACK when write, generate Error, do not continue the command list execute，generate IRQ 1: ignore NACK, when receive NACK, don't generate error, and will continue the command list execute	R/W	0x0

10.2.5.9 TWI_FIFOSTAT

TWI FIFO Status Register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:12	TFD	Tx FIFO level display This field indicate the current Tx FIFO level	R	0x0
11:8	RFD	Rx FIFO level display This field indicate the current Rx FIFO level	R	0x0
7	-	Reserved	R	0x0
6	WRS	Write or read status bit when acts as slave， used only in FIFO mode 0: master write to slave 1: master read from slave	R	0x0
5	TFF	TX FIFO full bit 0: not full 1: full	R	0x0
4	TFE	TX FIFO empty bit 0: not empty 1: empty	R	0x1
3	RFF	RX FIFO full bit 0: not full 1: full	R	0x0
2	RFE	RX FIFO empty bit 0: not empty 1: empty	R	0x1
1	RNB	Receive NACK Error bit 0: not receive NACK 1: receive NACK when write data	R/W	0x0

		Writing '1' to clear this bit		
0	CECB	Command Execute Complete bit 0: not complete 1: complete	R	0x1

10.2.5.10 TWI_DATCNT

TWI Data Transmit Counter Register
Offset=0x0024

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Data Transmit counter	R/W	0x0

10.2.5.11 TWI_RCNT

TWI Data Transmit Remain Counter Register
Offset=0x0028

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TC	Remain counter Displays the number of data not currently transmitted.	R	0x0

10.3 IRC

10.3.1 Features

- Support IRC receive function, include hardware mode, hardware self-learning mode, hardware awake mode, software decode mode, software awake mode
- Hardware mode support IRC transfer function, which support TC9012/NEC/RC5/RC6 protocol
- Need to connect an IR receiver when use
- Support remote infrared awake function

10.3.2 IRC Register List

Table 10-5 IRC Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
IRC	0xC0150000	0xC0150000

Table 10-6 IRC Registers Offset Address

Offset	Register Name	Description
0x0000	IRC_RX_CTL	Infrared remote control hardware interface control register
0x0004	IRC_RX_STAT	Infrared remote control hardware status register
0x0008	IRC_RX_ICC0	Infrared remote control hardware customer code register0
0x000C	IRC_RX_ICC1	Infrared remote control hardware customer code register1
0x0010	IRC_RX_ICC2	Infrared remote control hardware customer code register2
0x0014	IRC_RX_ICC3	Infrared remote control hardware customer code register3
0x0018	IRC_RX_RCC	Infrared remote control hardware customer data code register
0x001C	IRC_RX_IWKDC0	Infrared remote control hardware customer wake up key code 0 register
0x0020	IRC_RX_IWKDC1	Infrared remote control hardware customer wake up key code 1 register

0x0024	IRC_RX_IWKDC2	Infrared remote control hardware customer wake up key code 2 register
0x0028	IRC_RX_IWKDC3	Infrared remote control hardware customer wake up key code 3 register
0x002C	IRC_RX_KDC	Infrared remote control hardware customer key code register
0x0100	IRC_CTL	Infrared remote control software control register
0x0104	IRC_STAT	Infrared remote control software status register
0x0108	IRC_DAT	Infrared remote control software data register
0x010C	IRC_SCT	Infrared remote control software sample counter register
0x0110	IRC_TC	Infrared remote control software sample tolerance control register
0x0114	IRC_DB	Infrared remote control debounce register

10.3.3 IRC Register Description

10.3.3.1 IRC_RX_CTL

Infrared remote control hardware interface control register
Offset=0x0000

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7	MODE_SEL	IRC RX mode select 0: hardware mode 1: hardware self-learning mode	R/W	0x0
6	WFE	Wake up function enable bit 0: disable wake up function 1: enable wake up function	R/W	0x0
5	CCCD	customer code compare disable bit 0: enable customer code compare 1: disable customer code compare	R/W	0x0
4	KDCM	Key code compare disable bit 0: enable customer code compare 1: disable customer code compare	R/W	0x0
3	IRCE	IRC hardware enable 0: disable 1: enable	R/W	0x0
2	IIE	IRC hardware IRQ enable 0: disable 1: enable	R/W	0x0
1:0	ICMS	IRC coding mode select 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	R/W	0x0

10.3.3.2 IRC_RX_STAT

Infrared remote control hardware status register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15	DET_PRO_PD	Detect Protocol ok pending bit 0: detect protocol not ok 1: detect protocol ok	R/W	0x0

		Writing '1' to this bit will clear it		
14:13	PROTOCOL	Recognized Infrared Protocol 00: 9012 code 01: 8bits NEC code 10: RC5 code 11: RC6 code	R	0x0
12	-	Reserved	R	0x0
11	LDCM	Leader data code mismatch pending bit. Writing '1' to this bit will clear it, or auto clear if receive the correct leader data code the next time 0: leader data code match 1: leader data code mismatch	R/W	0x0
10:9	CCM	Customer code match 00: ICC0 customer match 01: ICC1 customer match 10: ICC2 customer match 11: ICC3 customer match	R	x
8	CCMP	Customer code mismatch pending 0: ICC customer match 1: ICC customer mismatch Writing '1' to this bit will clear it	R/W	0x0
7:6	IWKCDM	Key code match 00: IWKDC0 key match 01: IWKDC1 key match 10: IWKDC2 key match 11: IWKDC3 key match	R	x
5	IWKCDMP	IRC wake up key code mismatch pending bit 0: IWKDC key match 1: IWKDC key mismatch Writing '1' to this bit will clear it	R/W	0x0
4	RCD	Repeated code detected, Writing '1' to this bit will clear it, otherwise don't change 0: no repeat code 1: detect repeat code	R/W	0x0
3	WUP	Wake up pending bit 0: wake up pulse not generated 1: wake up pulse generated Writing '1' to this bit will clear it	R/W	0x0
2	IIP	IRC IRQ pending bit. Writing '1' to this bit will clear it 0: no IRQ pending 1: IRQ pending	R/W	0x0
1	-	Reserved	R	0x0
0	IREP	IRC receive error pending. 0: receive ok 1: receive error occurs if not match the protocol. Writing '1' to this bit will clear this bit, or auto clear if receive the correct user code and key data code the next time.	R/W	0x0

10.3.3.3 IRC_RX_ICC0

Infrared remote control hardware customer code register0
Offset=0x0008

Bits	Name	Description	Access	Reset

31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.4 IRC_RX_ICC1

Infrared remote control hardware customer code register1
Offset=0x000C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.5 IRC_RX_ICC2

Infrared remote control hardware customer code register2
Offset=0x0010

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.6 IRC_RX_ICC3

Infrared remote control(IRC) hardware customer code register3
Offset=0x0014

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Infrared remote control customer code In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R/W	0x0

10.3.3.7 IRC_RX_RCC

Infrared remote control hardware customer data code register
Offset=0x0018

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	CCRCV	customer code received In RC5 mode, Bit 4:0 is the customer code In 9012 mode, Bit 7:0 is the customer code, Bit 15:8 is the second customer code. The value is equal In 8 bit NEC mode, Bit 7:0 is the customer code, Bit 15:8 is the customer anti-code In RC6 mode, Bit 7:0 is the customer code.	R	0x0

10.3.3.8 IRC_RX_IWKDC0

Infrared remote control hardware customer wake up key code 0 register
Offset=0x001C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.9 IRC_RX_IWKDC1

Infrared remote control hardware customer wake up key code 1 register
Offset=0x0020

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.10 IRC_RX_IWKDC2

Infrared remote control hardware customer wake up key code 2 register
Offset=0x0024

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key	R/W	0x0

		anti-code In RC6 mode, Bit 7:0 is the key code.		

10.3.3.11 IRC_RX_IWKDC3

Infrared remote control hardware customer wake up key code 3 register
Offset=0x0028

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IWKDC	Infrared remote awake control key code In RC5 mode, Bit 4:0 is the key code In 9012 mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In 8 bit NEC mode, Bit 7:0 is the key code, Bit 15:8 is the key anti-code In RC6 mode, Bit 7:0 is the key code.	R/W	0x0

10.3.3.12 IRC_RX_KDC

Infrared remote control hardware customer key code register
Offset=0x002C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IKDC	IRC key data code In RC5 mode, Bit 5:0 is the Key data In 9012 and 8 bit NEC mode, Bit 7:0 is the Key data, Bit 15:8 is the Key anti-data In RC6 mode: Bit 7:0 is the Key data;	R	0x0

10.3.3.13 IRC_CTL

Infrared remote control software control register
Offset=0x0100

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11:4	SRL	Soft Select level Received data in ram Set the number of wake-up codes compared with those in RAM when using software wake-up mode.	R/W	0x40
3	SWCS	IRC wake up memory clk select bit 0: Hclk 1: Irc_clk	R/W	0x0
2	SWFE	Soft wake up function enable bit 0: disable wake up function 1: enable software wake up function	R/W	0x0
1	SIRCE	IRC software enable 0:disable 1:enable	R/W	0x0
0	SIIE	IRC software IRQ enable 0: disable 1: enable	R/W	0x0

10.3.3.14 IRC_STAT

Infrared remote software status register
Offset=0x0104

Bits	Name	Description	Access	Reset
31:13	-	Reserved	R	0x0
12	BUSY	IRC busy bit 0: busy 1: not busy	R	0x0
11:4	SRLV	IRC level in ram bit Current data IRC Ram received	R	0x0
3	SWUP	Wake up pending bit 0: wake up pulse not generated 1: wake up pulse generated Writing '1' to this bit will clear it	R/W	0x0
2	SIIP	IRC IRQ pending bit, Writing '1' to this bit will clear it. 0: no IRQ pending 1: IRQ pending	R/W	0x0
1	SIREP	IRC receive error pending 0: receive ok 1: receive error Error occurs when IRC ram overflows. Writing '1' to this bit will clear this bit.	R/W	0x0
0	SRST	IRC ram reset bit Writing '1' to reset IRC ram, auto clear to 0 when IRC ram reset complete.	R/W	0x0

10.3.3.15 IRC_DAT

Infrared remote control software data register
Offset=0x0108

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	IDAT	IRC data register	R/W	0x0

10.3.3.16 IRC_SCT

Infrared remote control software sample counter register
Offset=0x010C

Bits	Name	Description	Access	Reset
31:16	-	Reserved	R	0x0
15:0	ICCC	Receive Counter configure	R/W	0x0

10.3.3.17 IRC_TC

Infrared remote control software sample tolerance control register
Offset=0x0110

Bits	Name	Description	Access	Reset
31:7	-	Reserved	R	0x0
6:0	STC	When comparing the received sample count value with the data	R/W	0x0

		configured in RAM, the register can be used to configure the positive and negative error range in units of 5us.		

10.3.3.18 IRC_DB

Infrared remote control debounce register
Offset=0x0114

Bits	Name	Description	Access	Reset
31:9	-	Reserved	R	0x0
8	DBEN	Debouncer enable 0: disable 1: enable	R/W	0x0
7:0	DBC	Debouncer counter, 1 counter = 1/200KHz Default counter = 40(200us)	R/W	0x28

10.4 UART0 and UART1

10.4.1 Features

ATS2835P contains two UART interfaces: UART0 and UART1. UART0/1 has the following features:

- 5-8 Data Bits and LSB first in Transmit and Received
- 1-2 Stop Bits
- Even, Odd, or No Parity
- 16 Byte Transmit and Receive FIFOs
- Capable of speeds up to 6Mbps to enable connections with Bluetooth and other peripherals
- Support IRQ and DMA mode to transmit data
- Support RTS/CTS Automatic Hardware Flow Control to reduce interrupts to host system
- UART RX Support DMA single mode
- Add UART RX DMA counter for valid data in RAM。
- RX Baud Rate tolerance≤±2%
- UART0 TXFIFO can be accessed by CPU and DSP

10.4.2 UART0 Register List

Table 10-7 UART0 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART0	0xC0190000	0xC0190000

Table 10-8 UART0 Registers Offset Address

Offset	Register Name	Description
0x0000	UART0_CTL	UART0 Control Register
0x0004	UART0_RXDAT	UART0 Receive FIFO Data Register
0x0008	UART0_TXDAT	UART0 Transmit FIFO Data Register
0x000C	UART0_STA	UART0 Status Register
0x0010	UART0_BR	UART0 BAUDRATE divider Register

10.4.3 UART0 Register Description

10.4.3.1 UART0_CTL

UART0 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	RXENABLE	UART RX enable 0 : disable 1 : normal	R/W	0x0
30	TXENABLE	UART TX enable 0 : disable 1 : normal	R/W	0x0
29	TX_FIFO_EN	UART TX FIFO enable: 0: Disable 1: Enable	R/W	0x0
28	RX_FIFO_EN	UART RX FIFO enable: 0: Disable 1: Enable	R/W	0x0
27:26	TX_FIFO_SEL	UART TX FIFO Input Select 00: From CPU 01: From DMA 1x: From DSP	R/W	0x0
25:24	RX_FIFO_SEL	UART RX FIFO Input Select 00: From CPU 01: From DMA 1x: Reserved	R/W	0x0
23:21	-	Reserved	R/W	0x0
20	LBEN	Loop Back Enable. Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	R/W	0x0
19	TXIE	UART0 TX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
18	RXIE	UART0 RX IRQ Enable. 0: Disable 1: Enable	R/W	0x0
17	TXDE	UART0 TX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART0 RX DRQ Enable. 0: Disable 1: Enable	R/W	0x0
15	EN	UART0 Enable. When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	R/W	0x0
14	-	Reserved	R/W	0x0

13	RTSE	RTS Enable. When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: no request 1: request to send data	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART0 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (normal DMA), DO set 00 for 1 Bytes transfer for each DRQ.	R/W	0x0
9:8	TDIC	UART0 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable If this bit is 1, the transmitter checks CTS-before sending the next data byte. Note: this bit has no effect if autoflow enable bit is set. 0: do not checks CTS-before sending 1: checks CTS-before sending	R/W	0x0
6:4	PRS	Parity Select. Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	R/W	0x0
3	-	Reserved	R/W	0x0
2	STPS	STOP Select. If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated.	R/W	0x0

		0: 1 stop bit 1: 2 stop bit		
1:0	DWLS	Data Width Length Select. 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

10.4.3.2 UART0_RXDAT

UART0 Receive FIFO Data Register

Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	RXDAT	Received Data. The depth of FIFO is 8bit×16levels.	R	x

10.4.3.3 UART0_TXDAT

UART0 Transmit FIFO Data Register

Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TXDAT	Transmitted Data. The depth of FIFO is 8bit×16 levels	W	0x0

10.4.3.4 UART0_STA

UART0 Status Register

Offset=0x000C

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23	PAER	Parity Status 0: Parity OK 1: Parity error Writing '1' to the bit will clear the bit. When parity error.	R/W	0x0
22	STER	Stop Status 0: Stop OK 1: Stop error Writing '1' to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART0 TX busy bit 0: not busy, TX FIFO is empty and all data be shift out 1: busy	R	0x0
20:16	TXFL	TX FIFO Level The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level. The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty	R	0x1

		1: empty		
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty 1: Empty 0: No Empty	R	0x1
4	RXST	Receive Status 0: receive OK 1: receive error Writing '1' to the bit will clear the bit. When receive bit detect error, which would be parity error or clock error.	R/W	0x0
3	TFER	TX FIFO Error. 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the TX FIFO.	R/W	0x0
2	RXER	RX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the RX FIFO.	R/W	0x0
1	TIP	TX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear it.	R/W	0x0

10.4.3.5 UART0_BR

UART0 BAUDRATE divider register

Offset=0x0010

Bits	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27:16	TXBRDIV	UART0 TX BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28
15:12	-	Reserved	R	0x0
11:0	RXBRDIV	UART0 BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28

10.4.4 UART1 Register List

Table 10-9 UART1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
UART1	0xC01A0000	0xC01A0000

Table 10-10 UART1 Registers Offset Address

Offset	Register Name	Description
0x0000	UART1_CTL	UART1 Control Register
0x0004	UART1_RXDAT	UART1 Receive FIFO Data Register
0x0008	UART1_TXDAT	UART1 Transmit FIFO Data Register
0x000C	UART1_STA	UART1 Status Register
0x0010	UART1_BR	UART1 BAUDRATE divider Register

10.4.5 UART1 Register Description

10.4.5.1 UART1_CTL

UART1 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	RXENABLE	UART RX enable 0 : disable 1 : normal	R/W	0x0
30	TXENABLE	UART TX enable 0 : disable 1 : normal	R/W	0x0
29	TX_FIFO_EN	UART TX FIFO enable 0: Disable 1: Enable	R/W	0x0
28	RX_FIFO_EN	UART RX FIFO enable 0: Disable 1: Enable	R/W	0x0
27:26	TX_FIFO_SEL	UART TX FIFO Input Select 00: From CPU 01: From DMA 1x: From DSP	R/W	0x0
25:24	RX_FIFO_SEL	UART RX FIFO Input Select 00: From CPU 01: From DMA 1x: Reserved	R/W	0x0
23:21	-	Reserved	R/W	0x0
20	LBEN	Loop Back Enable Set this bit to enable a loop back mode that data coming on the input will be presented on the output. 0: Disable 1: Enable	R/W	0x0
19	TXIE	UART1 TX IRQ Enable 0: Disable 1: Enable	R/W	0x0
18	RXIE	UART1 RX IRQ Enable	R/W	0x0

		0: Disable 1: Enable		
17	TXDE	UART1 TX DRQ Enable 0: Disable 1: Enable	R/W	0x0
16	RXDE	UART1 RX DRQ Enable 0: Disable 1: Enable	R/W	0x0
15	EN	UART1 Enable When this bit is clear, the UART clock source is inhibited. This can be used to place the module in a low power standby state. 0:disable 1: enable	R/W	0x0
14	-	Reserved	R/W	0x0
13	RTSE	RTS Enable When this bit is set, request to send data. Note: This bit has no effect if Autoflow enable bit is set. 0: no request 1: request to send data	R/W	0x0
12	AFE	Autoflow mode Enable Setting this bit enables automatic hardware flow control. Enabling this mode overrides software control of the signals. 0: Autoflow mode disable (normal mode) 1: Autoflow mode enable	R/W	0x0
11:10	RDIC	UART1 RX DRQ/IRQ Control 00: set when RX FIFO received at least one byte data in IRQ/DRQ mode. 01: set when RX FIFO received 4 bytes data in IRQ mode 10: set when RX FIFO received 8 bytes data in IRQ/DRQ mode 11: set when RX FIFO received 12 bytes data in IRQ/DRQ mode In DMA burst mode (normal DMA), DO not set 00, 01 because at least 8 bytes necessary. In DMA single mode (normal DMA), DO set 00 for 1 Bytes transfer for each DRQ.	R/W	0x0
9:8	TDIC	UART1 TX DRQ/IRQ Control 00: set when TX FIFO is at least 1 byte empty in IRQ mode. 01: set when TX FIFO is 4 bytes empty in IRQ mode. 10: set when TX FIFO is 8 bytes empty in IRQ/DRQ mode. 11: set when TX FIFO is 12 bytes empty in IRQ/DRQ mode. In DMA mode, DO not set 00, 01 because at least 8 bytes necessary.	R/W	0x0
7	CTSE	CTS Enable If this bit is 1, the transmitter checks CTS-before sending the next data byte. Note: this bit has no effect if autoflow enable bit is set. 0: do not checks CTS-before sending	R/W	0x0

		1: checks CTS-before sending		
6:4	PRS	Parity Select Bit 6: PEN, Parity enable Bit 5: STKP, Stick parity Bit 4: EPS, Even parity PEN STKP EPS Selected Parity 0 x x None 1 0 0 Odd 1 0 1 logic 1 1 1 0 Even 1 1 1 logic 0	R/W	0x0
3	-	Reserved	R/W	0x0
2	STPS	STOP Select If this bit is 0, 1 stop bit is generated in transmission. If this bit is 1, 2 stop bits are generated. 0: 1 stop bit 1: 2 stop bit	R/W	0x0
1:0	DWLS	Data Width Length Select 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits	R/W	0x0

10.4.5.2 UART1_RXDAT

UART1 Receive FIFO Data Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	RXDAT	Received Data The depth of FIFO is 8bit×16levels.	R	x

10.4.5.3 UART1_TXDAT

UART1 Transmit FIFO Data Register
Offset=0x0008

Bits	Name	Description	Access	Reset
31:8	-	Reserved	R	0x0
7:0	TXDAT	Transmitted Data The depth of FIFO is 8bit×16 levels	W	0x0

10.4.5.4 UART1_STA

UART1 Status Register
Offset=0x000C

Bits	Name	Description	Access	Reset
31:24	-	Reserved	R	0x0
23	PAER	Parity Status 0: Parity OK 1: Parity error. Writing '1' to the bit will clear the bit.	R/W	0x0

		When parity error.		
22	STER	Stop Status 0: Stop OK 1: Stop error. Writing '1' to the bit will clear the bit. When stop bit detect error.	R/W	0x0
21	UTBB	UART1 TX busy bit 0:not busy, TX FIFO is empty and all data be shift out 1:busy	R	0x0
20:16	TXFL	TX FIFO Level The field indicates the current TX FIFO empty level.	R	0x10
15:11	RXFL	RX FIFO Level The field indicates the current RX FIFO level of valid data.	R	0x0
10	TFES	TX FIFO empty Status 0: no empty 1: empty	R	0x1
9	RFFS	RX FIFO full Status 0: no full 1: full	R	0x0
8	RTSS	RTS Status The bit reflects the status of the external RTS- pin.	R	0x0
7	CTSS	CTS Status The bit reflects the status of the external CTS- pin.	R	x
6	TFFU	TX FIFO Full 1: Full 0: No Full	R	0x0
5	RFEM	RX FIFO Empty 1: Empty 0: No Empty	R	0x1
4	RXST	Receive Status 0: receive OK 1: receive error Writing '1' to the bit will clear the bit. When receive bit detect error, which would be parity error or clock error.	R/W	0x0
3	TFER	TX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the TX FIFO.	R/W	0x0
2	RXER	RX FIFO Error 0: No Error 1: Error Writing '1' to the bit will clear the bit and reset the RX FIFO.	R/W	0x0
1	TIP	TX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear the bit.	R/W	0x1
0	RIP	RX IRQ Pending Bit 0: No IRQ 1: IRQ Writing '1' to the bit to clear it.	R/W	0x0

10.4.5.5 UART1_BR

UART1 BAUDRATE divider register
Offset=0x0010

Bits	Name	Description	Access	Reset
31:28	-	Reserved	R	0x0
27:16	TXBRDIV	UART1 TX BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28
15:12	-	Reserved	R	0x0
11:0	RXBRDIV	UART1 BAUDRATE divider BaudRate = Clock_source/BaudRate divider Clock_source = HOSC24M	R/W	0x28

10.5 SPI1

The SPI module is designed according to Motorola serial peripheral interface protocols. It can be configured as either a master or slave device. It can generate a large range of SPI clock so as to communicate with different devices supporting SPI protocols. Especially, this module support three operation mode: write & read, write only, read only mode.
SPI write & read mode use the MOSI pin to serially write instructions, addresses or data to the device. It also uses the MISO pin to read data or status from the device synchronous. This mode is designed to meet normal SPI application.

10.5.1 Features

- Support SPI normal mode: mode 0/1/2/3
- Only support normal 4 wire mode
- Support IRQ and DMA mode to transmit data
- Support D-cache Interface
- Support 16 level delay chain, 1ns/step
- Support 1x/2x/dual/4x/quad access SPI NOR
- Support slave mode
- Support 100MHz spi_clk as highest speed

10.5.2 SPI1 Register List

Table 10-11 SPI1 Registers Block Base Address

Name	Physical Base Address	KSEG1 Base Address
SPI1	0xC0110000	0xC0110000

Table 10-12 SPI1 Registers Offset Address

Offset	Register Name	Description
0x0000	SPI1_CTL	SPI1 Control Register
0x0004	SPI1_STA	SPI1 Status Register
0x0008	SPI1_TXDAT	SPI1 Transmit FIFO Data Register
0x000C	SPI1_RXDAT	SPI1 Receive FIFO Data Register
0x0010	SPI1_BC	SPI1 Byte Counter Register

10.5.3 SPI1 Register Description

10.5.3.1 SPI1_CTL

SPI1 Control Register
Offset=0x0000

Bits	Name	Description	Access	Reset
31	CLKSEL	FIFO write or read clock select 0: use CPU clock 1: use DMA clock	R/W	0x0
30	FWS	FIFO width select 0: 8bit 1: 32bit	R/W	0x0
29:28	SPI_MODE_SELECT	SPI Mode Select 00: Mode0 01: Mode1 10: Mode2 11: Mode3	R/W	0x3
27	DUAL_QUAD_SELECT	SPI1 Dual/Quad Mode Select It works only when SPI_IO_MODE select 2x IO mode or 4x IO mode 0: 2x/4x mode 1: dual/quad mode	R/W	0x0
26	RX_WRITE_SEL	SPI1 Rx Write Select, Select suitable cycle To sample the right rx data 0: delay 2 spi_clk cycle (used when SPI_DELAY <= 4'b1000) 1: delay 3 spi_clk cycle (used when SPI_DELAY <= 4'b1111)	R/W	0x0
25	DMS	DMA transmit mode select 0: burst8 mode 1: single mode	R/W	0x0
24	TXCEB	TX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
23	RXCEB	RX Convert Endian bit，only used in 32Bit mode: 0: not convert Endian 0x76543210 ->0x76543210 1: convert Endian 32bit mode: 0x76543210 ->0x10325476 When in 8 bit mode, this bit have no effect	R/W	0x0
22	MSS	Master or Slave mode select 0: Master mode 1: Slave mode	R/W	0x0
21	MSB	SPI LSB/MSB First Select 0: SPI transmit and receive MSB first 1: SPI transmit and receive LSB first	R/W	0x0
20	RILS	RX IRQ Level select	R/W	0x0

		0: RX FIFO not empty, generate IRQ 1: RX FIFO at least 8 level data, generate IRQ Note: this bit have no effect when SPI_RIRQ_EN is disable, SPI1_CTL[8].		
19:16	SPI_DELAY	SPI Master read clock delay time (valid when SPI_WR select write/read and read mode) 0000: no delay 0001: 1 unit delay 0010: 2 units delay 0011: 3 units delay 0100: 4 units delay 0101: 5 units delay 0110: 6 units delay 0111: 7 units delay 1000: 8 units delay 1001: 9 units delay 1010: 10 units delay 1011: 11 units delay 1100: 12 units delay 1101: 13 units delay 1110: 14 units delay 1111: 15 units delay	R/W	0x0
15	SPI_REQ	SPI Bus Request (AHB Interface Only, Please reference operation manual) 0:disable 1:enable	R/W	0x1
14	-	Reserved	R/W	0x0
13:12	TIME_OUT_CTRL	Time Out Control (Cache Interface Only) 00: Pull up the SS signal immediately after processing the current request 01: wait 32 cycles 10: wait 64 cycles 11: wait 128 cycles	R/W	0x0
11:10	SPI_IO_MODE	SPI data I/O mode select 00: 1x I/O mode select 01: 1x I/O mode select 10: 2x I/O mode select 11: 4x I/O mode select	R/W	0x0
9	SPI_TIRQ_EN	SPI TX IRQ Enable, trigger SPI TX IRQ when SPI TX FIFO at least 8 level empty 0: disable 1: enable	R/W	0x0
8	SPI_RIRQ_EN	SPI RX IRQ Enable, this trigger of SPI RX IRQ controlled by SPI1_CTL[20]. 0: disable 1: enable	R/W	0x0
7	SPI_TDRQ_EN	SPI TX DRQ Enable, trigger DRQ when SPI TX FIFO at least 8 level empty; When DMA remain counter < 8, trigger DRQ until all data transfer completely 0: disable 1: enable	R/W	0x0
6	SPI_RDRQ_EN	SPI RX DRQ Enable, trigger DRQ when SPI RX FIFO at least 8 level full; When DMA remain counter < 8, trigger DRQ until all data received completely 0: disable	R/W	0x0

		1: enable		
5	SPI_TX_FIFO_EN	SPI Tx FIFO Enable 0: Disable 1: Enable	R/W	0x0
4	SPI_RX_FIFO_EN	SPI Rx FIFO Enable 0: Disable 1: Enable	R/W	0x0
3	SPI_SS	SPI NSS pin control output 0: output low 1: output high	R/W	0x1
2	SPI_LOOP	SPI Master MOSI and MISO loopback enable (AHB Interface Only) 0: disable 1: enable	R/W	0x0
1:0	SPI_WR	SPI Read/Write Mode (AHB Interface Only) 00: disable 01: Read only 10: Write only 11: Read and Write	R/W	0x0

10.5.3.2 SPI1_STA

SPI1 Status Register
Offset=0x0004

Bits	Name	Description	Access	Reset
31:12	-	Reserved	R	0x0
11	TFWO	TX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
10	-	Reserved	R	0x0
9	RFWO	RX FIFO error pending if Write FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
8	TFRO	RX FIFO error pending if Read FIFO overflow occur 0: no error 1: error occur Writing '1' to clear this bit	R/W	0x0
7	SPI_RXFU	SPI1 RX FIFO Full 0: not full 1: full	R	0x0
6	SPI_RXEM	SPI1 RX FIFO Empty 0: not empty 1: empty	R	0x1
5	SPI_TXFU	SPI1 TX FIFO Full 0: not full 1: full	R	0x0
4	SPI_TXEM	SPI1 TX FIFO Empty 0: not empty 1: empty	R	0x1
3	SPI_TIRQ_PD	SPI1 TX IRQ Pending, Writing '1' to this bit will clear it. 0: No TX IRQ Pending	R/W	0x0